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New Evidence for Double Charged Oxide Trap of Submicron MOSFET's

Hiroshi NAKAMURA, Naoki YASUDA, Kenji TANIGUCHI and Chihiro HAMAGUCHI
Department of Electronics Engineering, Osaka University
2-1, Yamada-Oka, Suita City, Osaka 565, Japan

Akira TORIUMI
ULSI Research Center, Toshiba Corporation
1, Komukai, Saiwai, Kawasaki 210, Japan

Resistance fluctuations in very small-area MOSFET's are found to depend exponentially on temperature. Magnitude of the fluctuations is also proportional to the number of trapped electrons, implying the presence of a trap producing a localized modulation of the electrostatic potential near the Si/SiO_2 interface. The RTS with three levels is explained by the "*double charged oxide trap*" model.

1 Introduction

Low-frequency noise in MOSFET's due to thermally activated interface states has been a great concern as the size of LSI is miniaturized. For very small-area ($\leq 1\ \mu m^2$) MOSFET's, it may be expected to have only a few oxide traps in the vicinity of the Surface Fermi level over the entire channel region, which causes discrete current steps in the drain current resembling a random telegraph signal (RTS) [1-8]. Although it is generally believed that the RTS's are attributed to trapping events of individual inversion layer electrons at the oxide trap, the mechanism generating RTS is not well understood.

In this study, we present evidences that the discrete current steps are produced by the localized modulation of the electrostatic potential at the Si/SiO_2 interface. A full analysis of RTS with three levels is also presented and a "*double charged oxide trap*" model is proposed in order to explain the three-level RTS.

2 Experimental

The devices used were n-channel poly-Si gate MOSFET's with the effective channel dimensions of 1 μm length and 0.1~0.2 μm width. Gate oxide thickness is 20 nm. RTS's were measured in the range of the drain current from 10 nA to 1 μA at the drain voltage of 50 mV.

3 Results and Discussion

3.1 Current fluctuation due to charge trapping

For two-level current fluctuations of RTS's, it has been recognized that scattering of channel electrons due to a trapped electron brings about the reduction of the drain current [4]. The decrease in the drain current is caused by a decrease in both the surface mobility and the inversion charge density near the trap site: the trapped electron locally modulates electrostatic potential near the Si/SiO_2 inter-

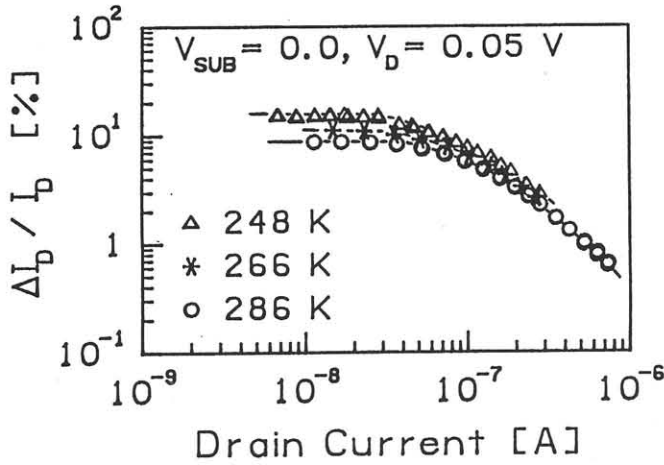


Fig. 1 Normalized drain current fluctuations as a function of drain current, with temperature as a parameter.

face and increases channel resistance over a small *"cored out"* area S of the channel. On the assumption of $WL \gg S$, a theoretically derived normalized current fluctuation is given by

$$\frac{\Delta I_D}{I_D} = \frac{1}{WL} \cdot (\pi r_s^2 + \frac{1}{n}), \quad (1)$$

where W is the channel width, L the channel length, n inversion charge density, r_s the effective radius of the cored out area S $(= \pi r_s^2)$. The first and the second terms of the right hand side represent the reduction in the effective channel area due to coulomb repulsive force and the number of channel electrons, respectively. For the drain current used in the experiments, the normalized current is directly proportional to the cored out area because the second term in Eq. (1) is much smaller than the first. In a weak inversion region, r_s is constant due to the lack of the screening, while in the strong inversion region (high current region), the screening due to the inversion charge controls the drain current, leading to the decrease in the normalized current. These characteristics are clearly observed in Fig. 1.

Figure 2 shows the normalized drain current fluctuations in a weak inversion region and theoretical size of the cored out region calculated by using the screened coulomb potential at the Si/SiO_2 interface, as a function of temperature. The screened coulomb potential in two-dimensional electron gas system is expressed as [9,10]

$$\phi(r, z) = \frac{Ze}{\kappa} \int_0^\infty \frac{q}{q + q_s} J_0(qr) \exp(-q|z_0|) dq, \quad (2)$$

where J_0 is a Bessel function of order zero and q_s the screening constant. z_0 and r are the distance of a trap from the interface and the distance along the interface. Z is the number of trapped electrons and κ is the effective dielectric constant. Since the size πr_s^2 of the cored out region depends on electron energy, the effective radius is evaluated by averaging over all electrons: both density of states and Fermi- Dirac statistics are taken into account. Using Eq. (2), one finds that the slope of the plots in Fig. 2 is almost independent of z_0. The calculated results exhibit exponential dependence on temperature and are qualitatively in good agreement with the experiments.

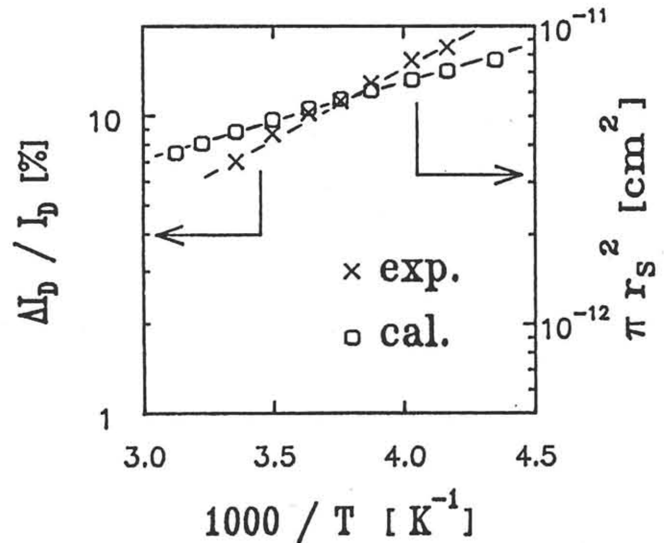


Fig. 2 Normalized drain current fluctuations in a weak inversion region and calculated *"cored out"* sizes as a function of temperature.

3.2 Capture and emission of electrons at an oxide trap

Figure 3 shows a typical example of RTS with three-level current fluctuations. For convenience, high,

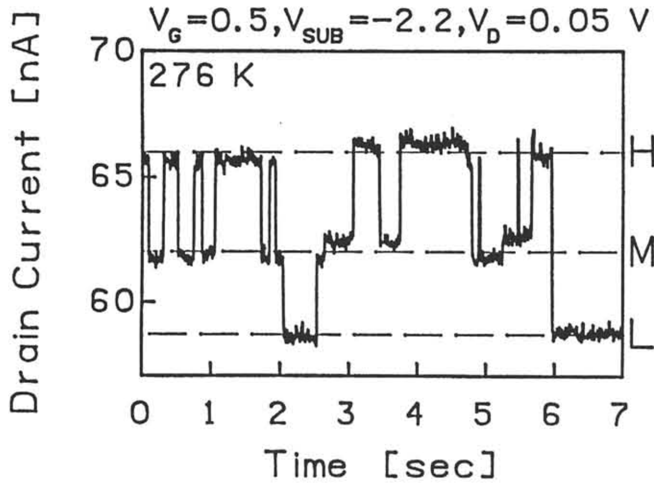


Fig. 3 Random telegraph signal with three-level current fluctuations.

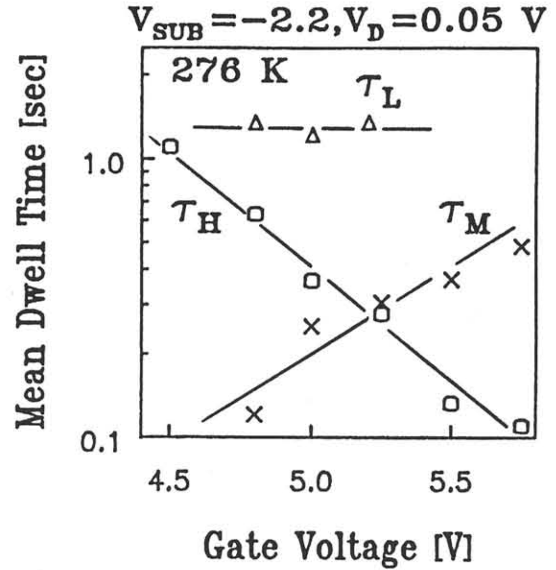


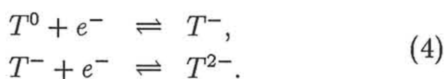
Fig. 4 Gate voltage vs. mean dwell time for three different current levels.

middle and low current levels are labeled as "H", "M" and "L", respectively. Fig. 4 shows mean dwell time in each current level as a function of gate voltage. The dwell times in "H" and "M" levels, τ_H and τ_M, are both strongly gate-voltage dependent (similar to gate-voltage dependence of dwell times in two-level RTS [1)]), while τ_L is independent. This can be explained by a model involving two- electron capture at a single trap. Fig. 5 shows the occupation probability of "M" and "L" levels as a function of gate voltage. Note that the slope of "L" level in low gate voltage is twice as large as that of "M", indicating the relation as

$$[L] \propto [M]^2, \tag{3}$$

where [ ] denotes the occupation probability of each trap state. The above relation is explained by the following "*double charged trap*" model.

Three symbols introduced to differentiate the charged states of a trap; T^0, T^- and T^{2-} correspond to none, single and double charged states, respectively. If electrons and trap are present simultaneously under thermal equilibrium conditions, they naturally react with each other according to



$$\begin{aligned} T^0 + e^- &\rightleftharpoons T^-, \\ T^- + e^- &\rightleftharpoons T^{2-}. \end{aligned} \tag{4}$$

The above relations imply dynamical equilibrium between capture and emission of electrons described by the mass action law as

$$\begin{aligned} [T^-] &\propto n \cdot (1 - [T^-] - [T^{2-}]), \\ [T^{2-}] &\propto n \cdot [T^-], \end{aligned} \tag{5}$$

where n is the inversion electron density. For low gate voltage, one can assume $[T^-]$, $[T^{2-}] \ll 1$. Therefore, one obtains the relation as

$$[T^{2-}] \propto [T^-]^2, \tag{6}$$

which is the same as Eq. (3). This indicates that the proposed double charged model accounts for the observed bias dependence of occupation probability as shown in Fig. 5. In addition, the double charged model is supported by comparing the experimental and the calculated step sizes among the three current levels. Figure 6 represents the calculated cored out sizes as a function of temperature for two different charged states. Note that the cored out size of double charged state is approximately twice as large as that of single charged state: the current step for "H"↔"M" transition is the same as that for "M"↔"L" transition.

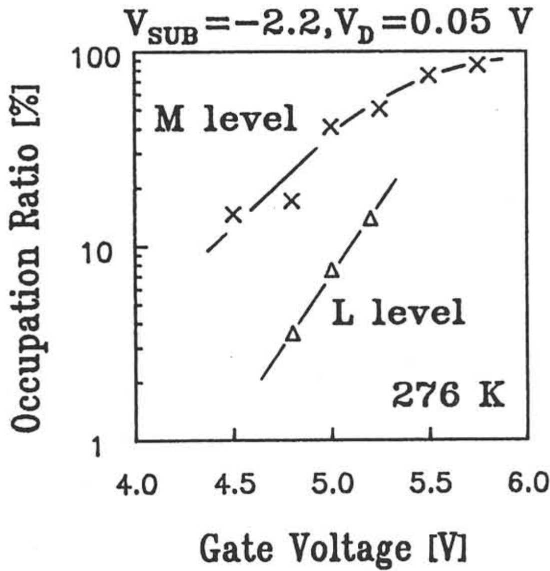


Fig. 5 Gate voltage vs. occupation probability of "*M*" and "*L*" levels.

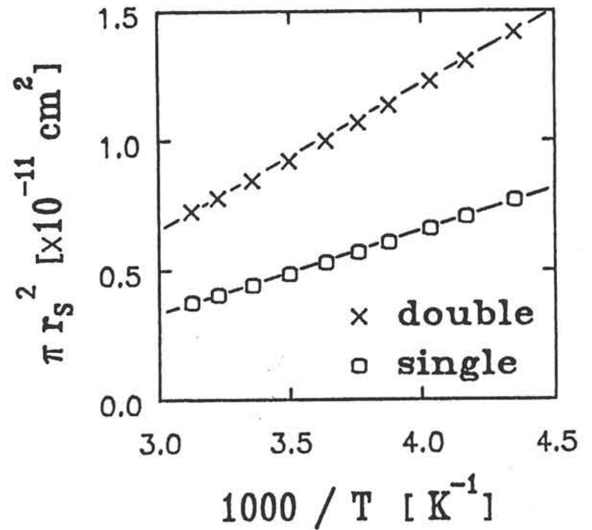


Fig. 6 Temperature vs. calculated cored out sizes for single and double charged states.

4 Conclusions

The channel current fluctuations observed in the submicron MOSFET's are found to be well explained by the modulation of the electrostatic potential due to the electron trapped in interface states. Magnitude of the fluctuations is proportional to the number of the trapped electrons. It is found that the current reduction due to the trapped electron greatly affects the mobility of inversion layer electrons. The effect of individual trapped charges becomes more important as device scaling continues: the accurate evaluation of the mobility of inversion layer electrons in small devices requires to involve these effects.

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