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Hot-Carrier Detrapping in Post-Stress Behavior of MOS Devices

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Detrapping phenomena in stressed MOS capacitors and transistors is observed by monitoring device characteristics after a constant current stress is applied. For the MOS capacitor, detrapping is manifested in the distinct "see-saw" behavior of the density of interface states, D_{it}. For the MOS transistor, detrapping is evidenced by the subsequent partial recovery of the threshold voltage. Threshold voltage recovery has two components, thermal recovery (TR) and field-assisted-recovery (FAR). Little measurable change in transconductance is observed after the removal of stress. These results suggest the occurrence of a degradation reversal which could be of importance in future device design.

1. INTRODUCTION

Hot-carrier-induced MOSFET degradation has been studied extensively due to its impact on the long-term reliability of VLSI devices and circuits. Much of the previous work has concentrated on the behavior of device characteristics such as V_{th} and g_m while a voltage stress is being applied. [1-5] In such cases, carrier trapping in the gate oxide and interface trap generation have been established as the mechanisms which cause the degradation to occur. After the stress is removed, it is expected that the device characteristics would recover at least partially. In this paper, we discuss post-stress results which reveal that degradation reversal occurs due to carrier detrapping. These results provide some insight into the mechanisms of carrier detrapping and trapped carrier redistribution.

2. EXPERIMENTAL PROCEDURE

MOS capacitors and MOS transistors are employed in this study. Capacitors have phosphorus-doped polysilicon gates with dimensions of 400μm x 153μm and 250μm x 400μm for n- and p- substrates respectively. Oxide thicknesses vary from 15nm to 20nm. NMOS and PMOS transistors have an effective channel length of 1.7μm and effective channel width of 99.4μm. The oxide thickness is 15nm and the gate electrode material is doped polysilicon. All transistors used are conventional single-drain devices.

Constant-current stress (Fowler-Nordheim injection) at fixed temperature is used to ensure that generated traps and trapped charges are uniformly distributed across the oxide cross-section, assuming edge effects can be neglected. In order to provide sufficient electrons for injection from p-type substrate, the sample is continuously illuminated throughout current stressing. Voltage versus time measurements are performed on capacitors with a current density of $5x10^{-5}$ A/cm^2 until a voltage shift of about 200 mV is obtained. C-V measurements are taken prior to stress and at time intervals subsequent to stressing. C-V curves are analyzed to obtain the D_{it} versus energy plot.[6] For quasi-static measurements, ramp rates of 50 mV/s and 10mV/s are used. Transistors are stressed for 1000 seconds with a current density of $6x10^{-5}$ A/cm^2. Post-stress electrical characteristics are then monitored for up to 10^4 seconds. V_{th} is determined at I_D=1μA. Maximum g_m is calculated in the linear region with V_D= 0.1V. The temperature dependence of the post-stress behavior is studied with threshold voltage and transconductance measurements between 81K and 373K.

3. RESULTS AND DISCUSSION

The increase in D_{it} due to current stressing approaches two orders of magnitude in both the n- and p- substrate capacitors. For the n-substrate capacitor, the "see-saw" effect ,[7] where the D_{it} peak positions and heights vary with post-stress time, is shown in Figure 1a. Unlike the see-saw observed in radiation-damaged capacitors,[8] where atomic rearrangements can be expected, the see-saw resulting from current stressing is most likely caused by carrier detrapping and repopulation in generated trap states. Such a mechanism would create significant charge redistribution, hence the see-saw in D_{it}. At 173K, this thermally activated process is less likely to occur, hence the small variations in post-stress D_{it} as shown in Figure 1b. Figure 2 shows ΔD_{it} evaluated at maximum post-stress D_{it} with temperature as a parameter. The change in D_{it} over time is substantially larger at higher temperatures. This is consistent with the notion that carrier repopulation among trap states is less probable at lower temperatures. From Figure 2, a ΔD_{it} versus 1/T plot yields a carrier repopulation activation energy of 80meV.

Figure 3 shows post-stress ΔV_{th} and Δg_m behavior of the transistors. The fractional change in g_m is very

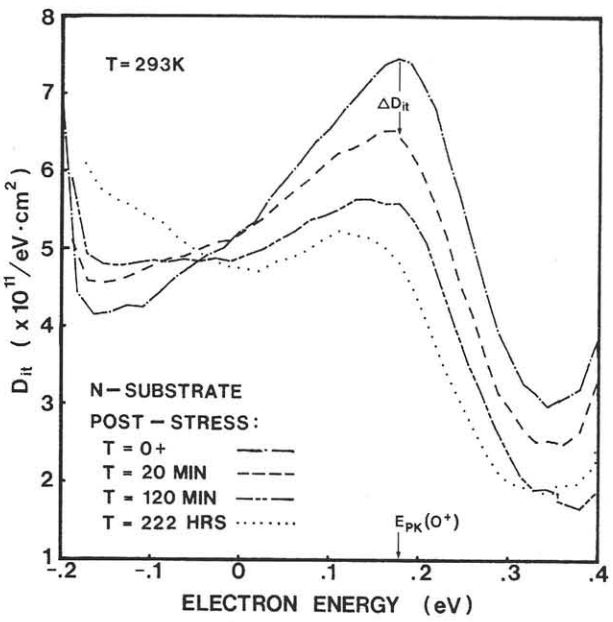

Figure 1a. Density of interface states vs. electron energy at T=293K. Zero energy corresponds to mid-gap.

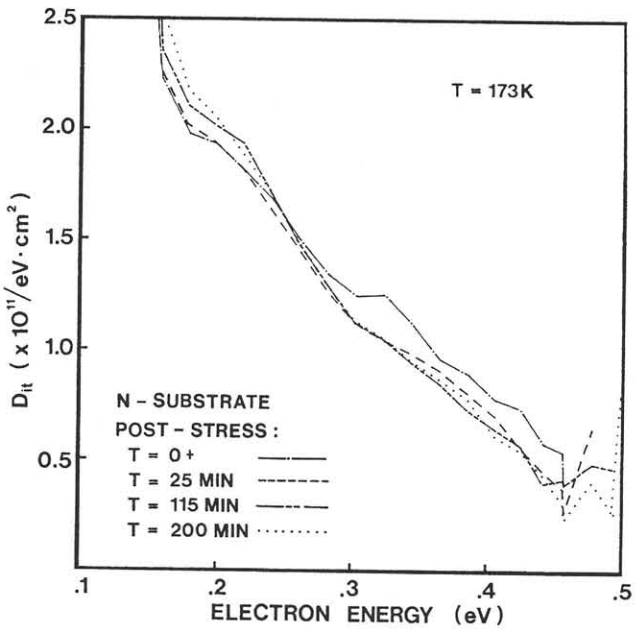

Figure 1b. Density of interface states vs. electron energy at T=173K.

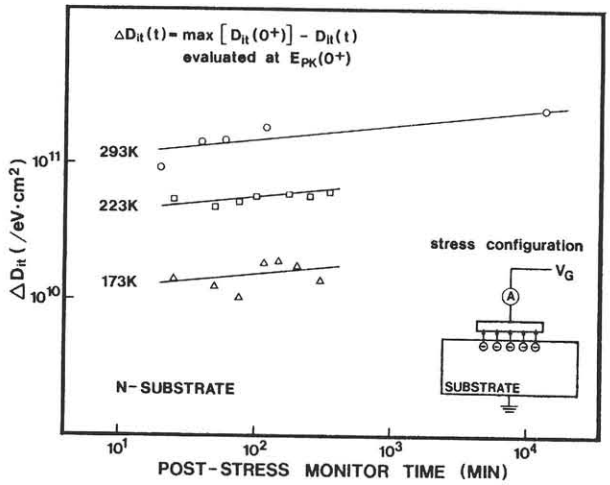

Figure 2. ΔD_{it} evaluated at constant electron energy with temperature as a parameter. Energy is chosen at $D_{it}^{PK}(t=0^+)$.

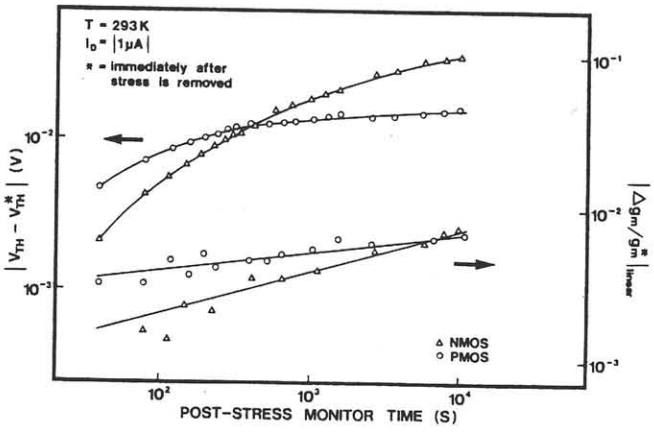

Figure 3. Post-stress ΔV_{th} and g_m behavior.

small, i.e. less than 1% whereas changes in threshold voltage are in the tens of millivolts range. Since the effect of carrier trapping on V_{th} is generally more pronounced than that on g_m,[2] the effect of carrier detrapping is more pronounced as well. ΔV_{th} shows rapid recovery initially. Such kinetics can also be observed in Figure 1 where a larger change in D_{it} occurs at the early post-stress stages.

For the PMOS devices, temperature dependence of the post-stress ΔV_{th} with no applied gate bias is shown in Figure 4. Similar curves are obtained for NMOS. ΔV_{th} decreases with decreasing temperature, consistent with the capacitor data of Figure 2 where smaller changes in D_{it} occur at lower temperatures. By plotting ΔV_{th} versus 1/T, an activation energy, E_{DTR}, of 63 meV is obtained (Figure 5). E_{DTR} corresponds to a thermal detrapping activation energy for spontaneous recovery. This value is consistent with the carrier repopulation activation energy obtained for the MOS capacitor.

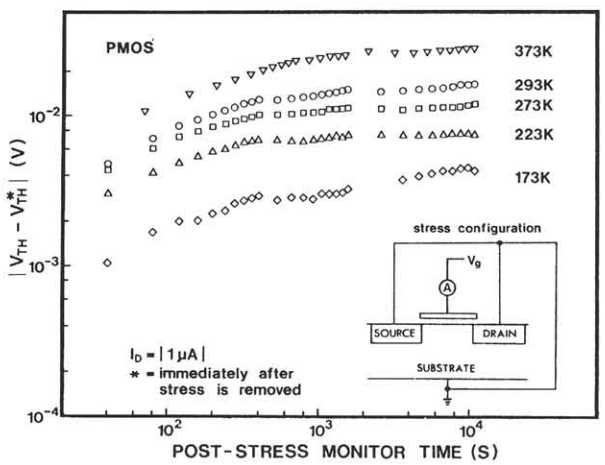

Figure 4. Post-stress ΔV_{th} behavior for PMOS transistors with temperature as a parameter.

Experiments performed at fixed temperature with varying gate bias yield the FAR component of the threshold voltage shift. For the PMOS transistor, the gate voltage dependence of the post- stress ΔV_{th} is shown in Figure 6. Similar curves are obtained for the NMOS transistor. Application of a positive V_G results in substantially less threshold voltage recovery. In the negative V_G regime, three regions can be identified (Figure 7). At low gate bias, TR is more dominant than FAR. Between -2V and-10V, the vertical oxide field at and near the interface promotes carrier detrapping, thus resulting in enhanced recovery. For each region, ΔV_{th} assumes the form $\Delta V_{th}=\Delta V_{tho}\cdot\exp\left(-\frac{C}{V_G}\right)$, with a different constant C. At $|V_G|$ greater than 10V, the substrate band bending near the interface is considerable, which could give rise to trap-to-band tunneling. Such tunneling can result in further recovery enhancement.

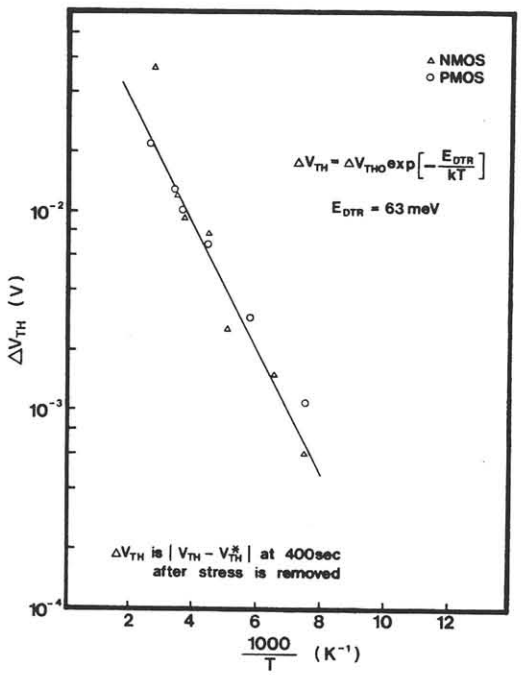

Figure 5. Post-stress ΔV_{th} versus 1/T plot.

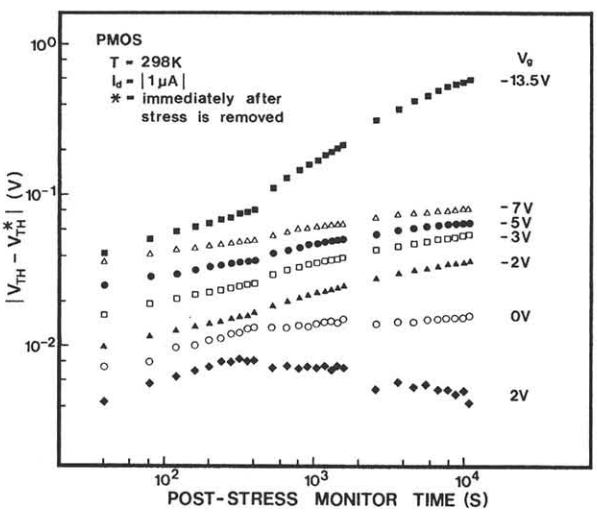

Figure 6. Post-stress ΔV_{th} behavior for PMOS transistors with gate bias as a parameter.

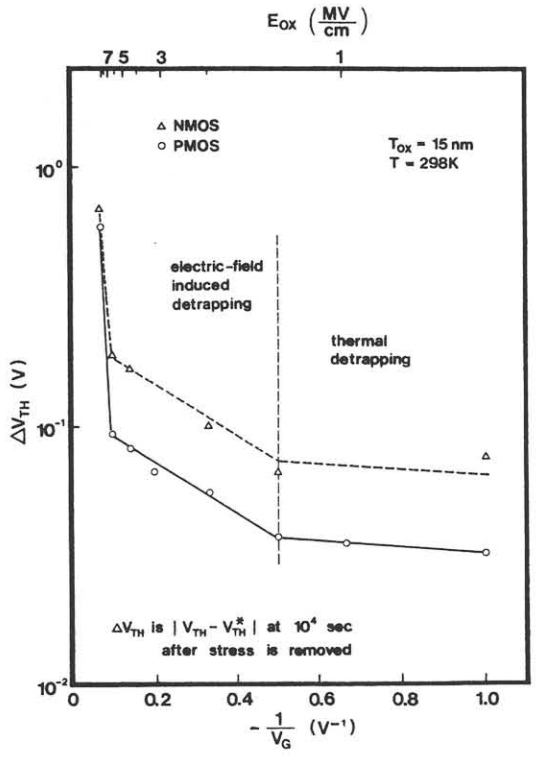

Figure 7. Post-stress ΔV_{th} versus $1/V_G$ plot.

4. CONCLUSION

Detrapping phenomena in stressed MOS devices is observed by monitoring device characteristics at different temperatures. The ΔV_{th} activation energy obtained for transistors is similar to the trapped carrier repopulation activation energy of the MOS capacitor. This leads us to believe that the thermal component of the threshold voltage recovery is due to carrier detrapping and repopulation. Threshold voltage recovery can be enhanced with suitable gate bias. Total threshold voltage recovery can be expressed as the sum of the TR and FAR components, $\Delta V_{th}=\Delta V_{th}^{T}+\Delta V_{th}^{F}$. For large negative gate bias in NMOS, recovery is probably due to trap-to-band tunneling and is considerable. This suggests a means for prolonging the lifetimes of submicron devices. Results of post-stress measurements can serve as the basis for further study of hot-carrier-induced degradation and recovery mechanisms. In addition, this detrapping effect will be correlated with AC stress measurements.

5. REFERENCES

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