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Hot Carrier Degradation of 0.5 μm Surface and Buried Channel PMOS FETs

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This paper presents the comparison of hot carrier degradation between the surface (P^+poly gate) and the buried (N^+poly gate) channel PMOS transistors. Simulation and experimental results show that the drain electric field of the surface channel is higher than that of the buried channel. On the contrary, the buried channel have a higher injection ratio of avalanche hot electrons into the gate as compared with that of the surface channel due to the work function difference. Thereby the life time of the surface channel is comparable with that of the buried channel. It is also shown that the life time of the 0.5μm surface channel PMOSFET can be as long as 10 years under the supply voltage of 5V, employing the LDD structure.

INTRODUCTION

There has been a growing interest in surface channel PMOSFET with P^+poly gate for CMOS VLSI of 0.5μm or shorter channel length due to the superior short channel behavior, compared with the buried channel PMOSFET with N^+poly gate [1-2]. However little has been known for hot carrier degradation of the surface channel PMOS in comparison with many reports of the buried channel [3-7]. Therefore this paper reports on the comparison of hot carrier degradation between the surface and buried channel LDD PMOSFET.

FABRICATION PROCEDURE

Surface and buried channel PMOS transistors were fabricated as follows.
Phosphorus ions were implanted into the channel region for threshold voltage adjustment of the surface channel while boron and arsenic ions were doubly implanted for the buried channel to form a shallow buried layer to suppress the short channel effect.
After gate oxidation with thickness of 15nm, undoped and phosphorus-doped polysilicon were deposited for the surface and the buried channel, respectively. After gate delineation, boron ions were implanted to form lightly doped source/drain. Subsequently sidewall spacer was formed.
Afterwards boron ions were implanted to form the P^+ source/drain as well as to dope the undoped polysilicon gate simultaneously into P-type in the case of the surface channel.

RESULTS AND DISCUSSION

Figure 1 presents the simulation results of avalanche hot carrier generation rate for the surface and the buried channel PMOSFET under the maximum substrate current conditions. Due to the electric field concentration in the vicinity of P-N junction at the drain edge, the surface channel PMOS shows the generation rate higher than the buried channel with no P-N junction between the channel and the drain. However the buried channel PMOS have higher normal electric field which favors electron injection into the gate, compared with the surface channel as shown in the simulation results of Fig.2. This is due to the work function difference of gate materials between the two.

In support of the simulation results, experimental results in Fig.3 show that the surface channel PMOSFETs at various gate length have larger values of the substrate current/the drain current related to the drain electric field as compared with the buried channel. Figure 3 also shows the injection ratio of avalanche hot carriers into the gate, expressed by the maximum gate current/the substrate current for the surface and the buried channel PMOSFETs. The injection ratio of the buried channel is larger than that of the surface channel as explained by the normal electric field in Fig.2.

Figure 4 shows the dependence of both the gate current and the substrate current on the drain voltage for the surface and the buried channel PMOSFETs. For prepared samples, both the surface channel and the buried channel PMOSFETs have approximately the same gate current values over various drain voltage, while the surface channel shows larger substrate current than the buried channel.

Hot carrier degradation was investigated as a function of gate voltage at the supply voltage of -8V as well as gate voltage dependence of substrate and gate currents as shown in Fig.5. After the stress of 10^3 seconds, the drain current shift was measured in the reverse mode. Though the substrate current of the surface channel is larger than that of the buried channel, the peak drain current shifts in the triode and the pentode for the surface channel are almost equal to those for the buried channel. This can be explained by the difference in the injection efficiency of avalanche hot electrons into the gate between the surface and the buried channel PMOSFETs due to the gate work function difference as previously explained.

Threshold voltage and drain current shift were measured in the triode and the pentode region by the forward mode as well as by the reverse mode for surface channel PMOSFETs as presented in Fig.6 and Fig.7. In the triode region, the shifts are almost identical for the forward and the reverse mode. However in the pentode region, the drain current shift in the forward mode is larger than that in the reverse mode in contrast to the larger threshold voltage shift in the reverse mode. This larger drain current shift in the forward mode of the pentode region can be ascribed to the emphasized effect of reduced effective channel length. It should be also noted that the threshold voltage shift in the pentode region is larger than that in the triode region which is again explained by the drain induced barrier lowering effect due to the decreased effective channel length by electron traps.

Hot carrier degradation was compared between LDD and non LDD for the surface channel PMOS. As presented in Fig.8, the drain electric field can be reduced by employing the LDD structure. The life time of the surface channel LDD and non LDD are shown as a function of supply voltage in Fig.9. Here the life time is defined as the time to reach 10% of the drain current shift measured in the reverse mode. It should be noted that the surface channel LDD PMOS can have the life time longer than 10 years at the supply voltage of 5V.

CONCLUSION

Simulation and experimental results show that the drain electric field of the surface channel is higher than that of the buried channel. On the contrary, the buried channel have a higher injection ratio of avalanche hot electron into the gate as compared with that of the surface channel due to the gate work function difference, thereby resulting in the life time of the surface channel comparable with or longer than that of the buried channel. The life time of the surface channel can be as long as 10 years under the supply voltage of 5V with the use of the LDD structure.

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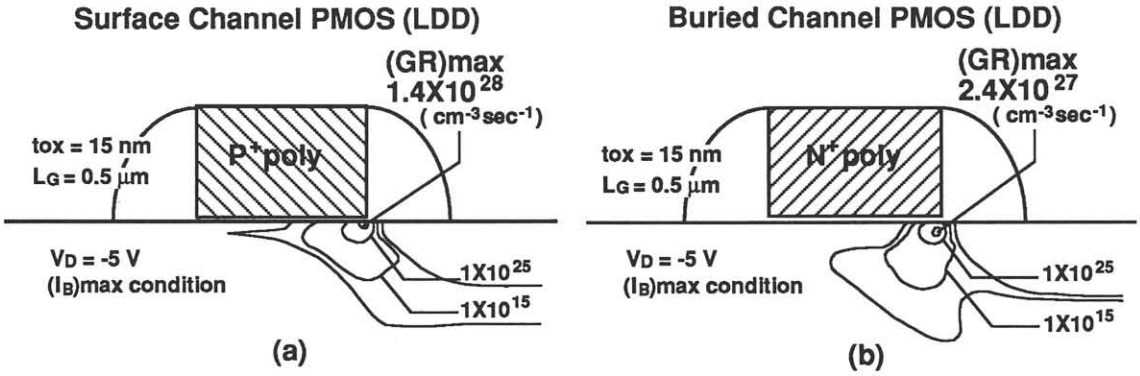


Fig.1 : Simulated hot carrier generation rate
(a): Surface Channel PMOS (LDD), (b): Buried Channel PMOS (LDD)

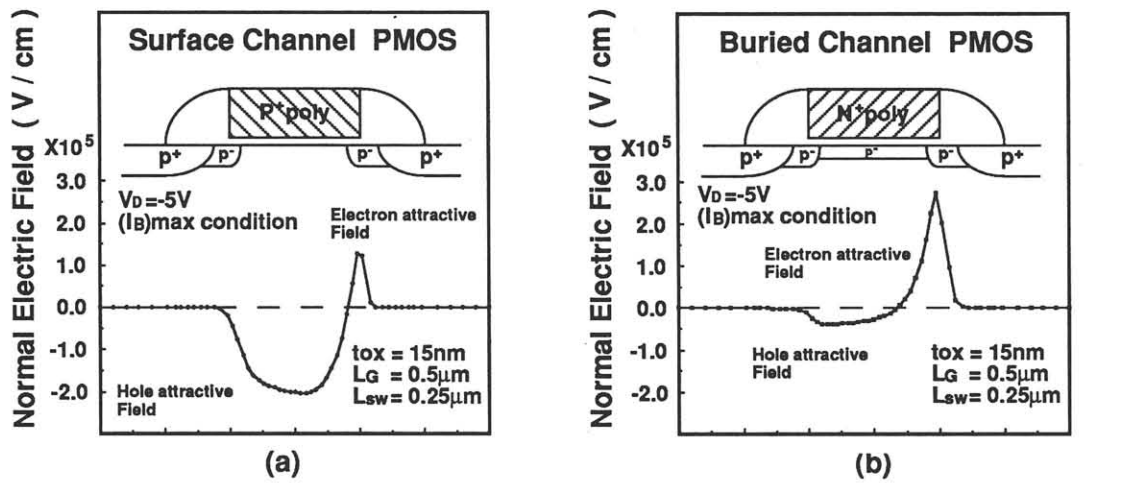


Fig.2 : Normal Electric Field at Si-SiO_2 Interface. (a) : Surface Channel PMOS, (b) : Buried Channel PMOS

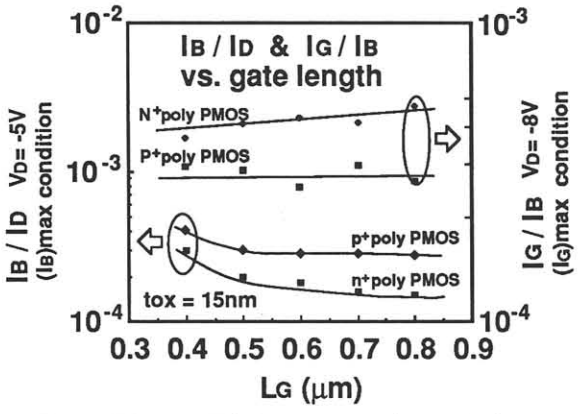


Fig.3 : Substrate / drain current and gate / substrate current as a function of gate length

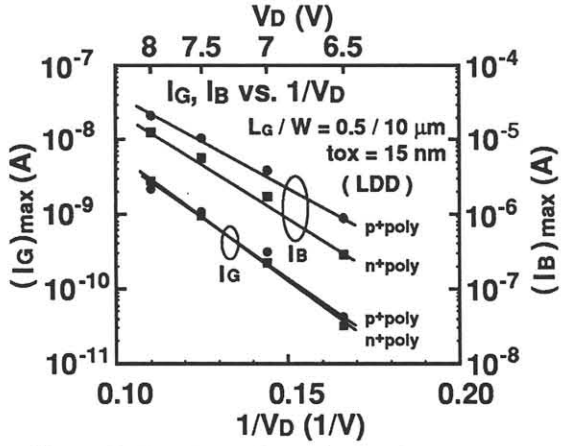
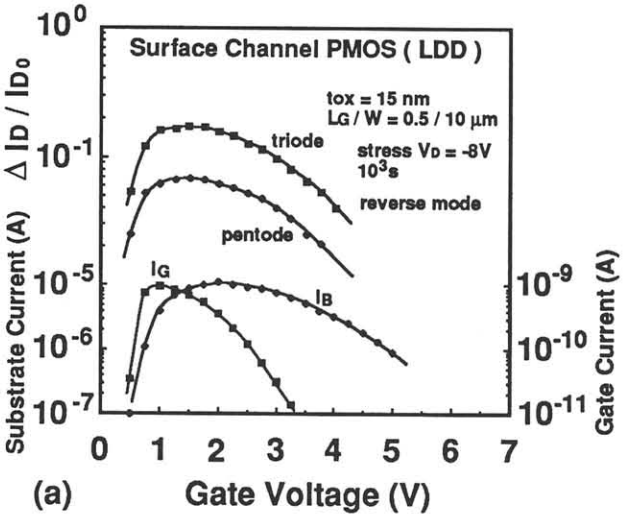


Fig.4 : Drain voltage dependence of gate current and substrate current



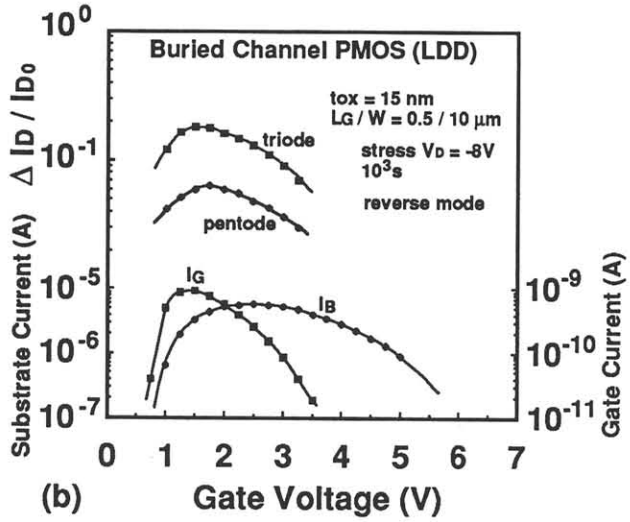


Fig.5 : Gate voltage dependence of drain current shift (a) : Surface Channel PMOS, (b) : Buried Channel PMOS

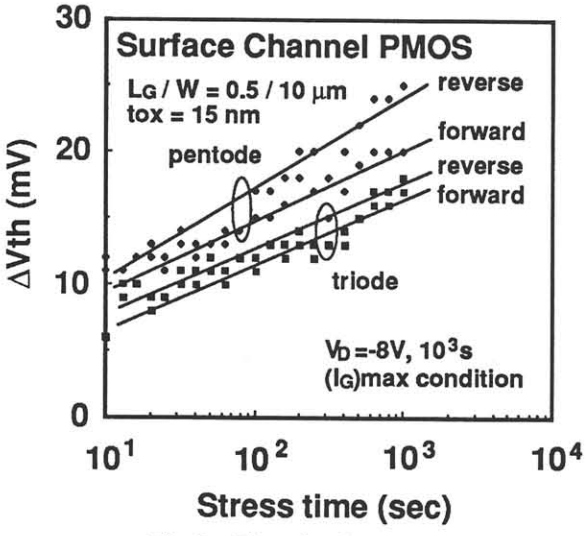


Fig.6 : Threshold voltage shift.

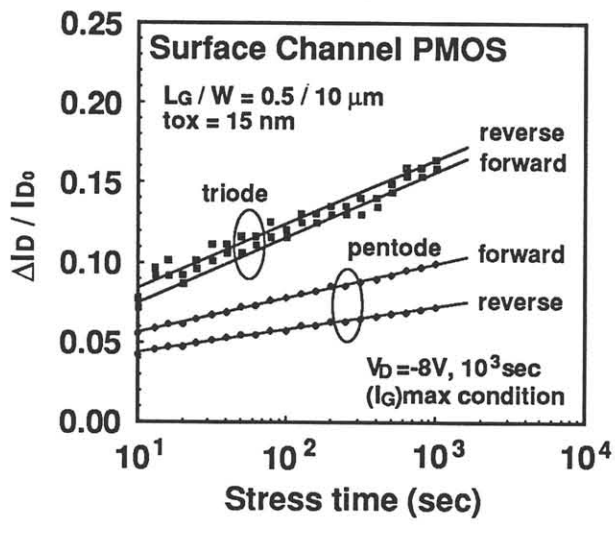


Fig.7 : Drain current shift.

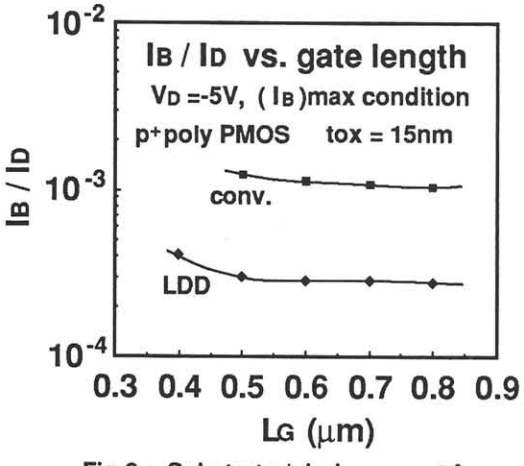


Fig.8 : Substrate / drain current for various gate length

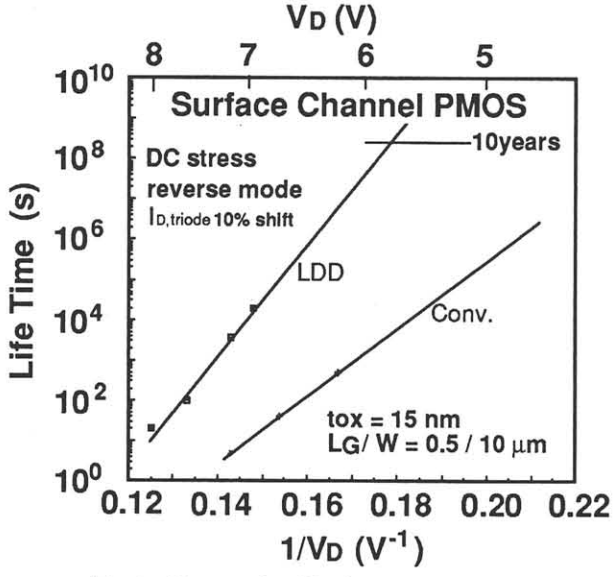


Fig.9: Hot carrier life time vs. supply voltage.