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Mechanism Analysis of a Highly Reliable Graded Junction Gate/N^- Overlapped Structure in MOS LDD Transistor

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A newly developed gate/N^- overlapped MOS LDD transistor has been investigated. The transistor was fabricated by oblique rotating ion implantation technique. A new formula of impurity ion profile was derived theoretically to analyze the lowering of substrate current and improvement of the degradation caused by hot-carrier effect of the transistor. As the results, it was proved that impurity ion profile near the drain edge is remarkably graded even just after the implantation, so that maximum electric field is remarkably relaxed as compared with conventional transistor. And also the maximum point of lateral electric field at the drain edge is located apart from the main path of channel current and is located under the gate electrode. This tendency turned out to be promoted with increase of oblique angle and energy of implanted ions.

1. Introduction

One of the most important problems for submicron transistors is to improve hot-carrier lifetime without the degradation of current drivability.

Recently, Mayaram et al. first pointed out that a gate/N^- overlapped structure gives high relaxation in electric field at the drain edge of LDD transistor.[1)-2)] After that, some analytical and experimental studies verified that the gate/N^- overlapped structure is effective to solve the above problem.[3)-8)] However, the gate/N^- overlapped structure fabricated by oblique rotating ion implantation technique has not been analyzed sufficiently.

In this paper, the newly developed gate/N^- overlapped MOS LDD transistor has been investigated. The transistor was fabricated by oblique rotating ion implantation technique. First, the dependence of characteristics of the new LDD transistor on process parameters of oblique rotating ion implantation was examined. Secondly, hot-carrier-induced degradation in dynamic RAMs having the new LDD transistor was measured on low temperature operational test. Finally, deriving the new theoretical model, mechanisms of lowering of substrate current and improvement of the degradation caused by hot-carrier effect of the new LDD transistor have been analyzed.

2. Experiments and results

Figure 1 shows schematic view of the oblique rotating ion implantation. N-channel LDD MOS transistor having gate length of 0.9μm and gate width of 10μm was fabricated. Gate electrode of 200nm thick polysilicon with upperlayered 100nm thick oxide was formed on 20nm thick gate oxide. The width of side-wall oxide was 0.3μm. Phosphorus ion was used to form N^- region by oblique rotating ion implantation, including conventional fixed 0° ion implantation as a reference. And arsenic ion was used to form N^+ region by conventional fixed 7° ion implantation with its dose of $4.0E15cm^{-2}$.

Figure 2 shows the dependence of substrate current (Ib), ratio of Ib and drain current (Ids), threshold voltage (Vth), source/drain breakdown voltage (BVds), Ids and delay time of ring oscillator per step

(tpd) on oblique angle (θ). Energy and dose of N^- implantation conditions were 30/cosθ(KeV) and 2.0E13/cosθ (cm^{-2}), respectively, where θ=0, 15, 30, 45 and 60°. Both Ib and Ib/Ids decrease drastically with increase of θ. While changes of the other characteristics such as Vth, BVds, Ids, and tpd are much smaller than those of Ib and Ib/Ids.

We examined the long-term degradation of 4M bit DRAMs having the new LDD transistor on low temperature operational test. The implantation conditions to form gate/N^- overlapped structure were the same as mentioned above. Applied voltage and operating temperature of the test were Vcc=8V and Ta=-20°C, respectively. The test was carried on up to 300 hours. The shifts of device parameters such as RAS access time (tRAC) and CAS access time (tCAC) have not been observed on the samples except 0° implantation.

3. Theoretical formulation

In order to explain the above results, we derived a new theoretical formula of impurity ion profile formed by the oblique rotating ion implantation. Such a theoretical formula was first derived by Eimori, et al.[4] However, It took account of only a simplified shadowing effect of gate electrode for implanted ions. Their model neglects oblique incidence correction of ions into the substrate. In order to calculate impurity ion profile more precisely, following three important and inherent factors in the oblique rotating ion implantation must be discussed.

(A) the shadowing of gate electrode for implanted ions containing the oblique incidence correction.
(B) the entering of implanted ions under the gate electrode edge.
(C) the penetration of implanted ions through the polysilicon at the gate edge.

Especially, the factors of (B) and (c) are indispensable to analyze the gate/N^- overlapped structure.

Taking account of these three factors, we derived a theoretical formula of impurity ion profile. Here, the LSS theory with the approximation that projected standard deviation is nearly equal to lateral standard deviation was used. Setting up the coordinates system as shown in Fig.3, we obtained the explicit expression of the impurity ion profile, as follows;

$$N(X,Z;\Delta x,\Delta Rp,Rp;h_1,h_2,\theta)$$

$$=N_0^-\cos\theta\{W(X;\Delta x,\alpha,\beta)\rho(Z-\gamma;\Delta R_p)+W_{mod}(X;\Delta x,\Delta R_p,\beta,\gamma;h_2)\rho_{mod}(Z;\Delta Rp,\gamma;h_2)\}$$

where

$$W(X;\Delta x,\alpha,\beta)=\phi(X+\beta;\Delta x)-\psi_1(X;\Delta x,\alpha)-\psi_2(X;\Delta x,\beta)$$

$$W_{mod}(X;\Delta x,\Delta R_p,\beta,\gamma;h_2)=C(\Delta R_p,\gamma;h_2)\tan\theta F_{mod}(X;\Delta x,\beta)$$

$$\rho_{mod}(Z;\Delta R_p,\gamma;h_2)=C^{-1}(\Delta R_p,\gamma;h_2)G_{mod}(Z;\Delta R_p,\gamma;h_2)$$

and

$$F_{mod}(X;\Delta x,\beta)=\rho(-X-\beta;\Delta x)-\rho(-X;\Delta x)/2+\psi_{mod}(X;\Delta x,\beta)$$

$$G_{mod}(Z;\Delta R_p,\gamma;h_2)=\phi(Z-\gamma+h_2;\Delta R_p)-\phi(Z-\gamma;\Delta R_p)$$

$$C(\Delta R_p,\gamma;h_2)=\int_0^{+\infty}dZG_{mod}(Z;\Delta R_p,\gamma;h_2)$$

$$\psi_1(X;\Delta x,\alpha)=(1/\pi)\int_{-\infty}^{-x+\alpha}du\cos^{-1}\{(u+X)/\alpha\}\rho(u;\Delta x)$$

$$\psi_2(X;\Delta x,\beta)=(1/\pi)\int_{-X-\beta}^{-X}du\cos^{-1}\{(u+X)/\beta\}\rho(u;\Delta x)$$

$$\psi_{mod}(X;\Delta x,\beta)=(1/\pi)\int_{-X-\beta}^{-X}du\cos^{-1}\{(u+X)/\beta\}\{-u\rho(u;\Delta x)/(\Delta x)^2\}$$

$$\rho(a;b)=(1/\sqrt{2\pi}b)\exp(-a^2/2b^2)$$

$$\phi(c;b)=\int_{-\infty}^{c}da\rho(a;b)$$

and

$$\alpha=(h_1+R_p\cos\theta)\tan\theta$$

$$\beta=(R_p\cos\theta)\tan\theta$$

$$\gamma=R_p\cos\theta$$

Here, Rp, ΔRp and Δx are projected range, projected standard deviation and lateral standard deviation, respectively. These factors depend on energy of implanted ions (Eimp). N_0^- is dose of N^- implanted ions. h1 and h2 are the heights of gate electrode with and without upperlayered oxide, respectively.

The weight function of W(X;Δx,α,β) de-

scribes both the shadowing effect of gate electrode for implanted ions and the entering effect of implanted ions under the gate electrode. And the weight function of $W_{mod}(X;\Delta x,\Delta Rp,\beta,\gamma;h2)$ describes the penetrating effect of implanted ions through the polysilicon at the gate electrode edge. The impurity ion profiles of $\rho(Z-\gamma;\Delta Rp)$ and $\rho_{mod}(Z;\Delta Rp,\gamma;h2)$ are normalized to unit.

4. Numerical calculations and Simulations

We carried out numerical calculation and simulation for nMOS transistor having the gate length of 0.8μm, the gate oxide thickness of 18nm, the gate height (h1) of 300nm and the side-wall width of 0.3μm. The h1 is assumed to be equal to h2 for simplicity.

Figure 4 shows the results of numerical calculations of $W(X)$, $W_{mod}(X)$, $\rho(Z)$ and $\rho_{mod}(z)$ for implantation conditions of $\theta=45°$, Eimp=42KeV and $N_0^-=2.8E13cm^{-2}$. From Fig.4, it was found that the entering factor (B) and the penetration factor (c) are not negligible. Therefore, impurity ion profile under the gate electrode resulting from the factors of (B) and (c) was proved to be important. In addition, the profile turned out to be remarkably graded even just after the implantation. N^-/p junction becomes more graded after total heat treatment.

Figure 5 shows the calculated results of carrier concentration and lateral electric field near the drain edge for implantation conditions of $\theta=45°$, Eimp=42KeV and $N_0^-=2.8E13cm^{-2}$. And implantation conditions of $\theta=0°$, Eimp=30KeV and $N_0^-=1.0E13cm^{-2}$ was employed as a reference. Applied voltages to drain, gate, source and substrate were Vd=7.0V, Vg=3.0V, Vs=0.0V and Vb=-3.0V. From Fig.5, it was proved that the maximum point of lateral electric field at the drain edge is located apart from the main path of channel current and is located under the gate electrode. This tendency turned out to be more promoted with increase of oblique angle and energy of implanted ions.

5. Conclusions

The new formula of impurity ion profile formed by the oblique rotating ion implantation was derived theoretically. It contains three important and inherent factors in the oblique rotating ion implantation, that is, the shadowing of gate electrode for implanted ions, the entering of implanted ions under the gate electrode edge and the penetration of implanted ions through the polysilicon at the gate electrode edge. Mechanisms of lowering of substrate current and improvement of the degradation caused by hot-carrier effect have been analyzed theoretically. As the results, it was proved that impurity ion profile near the drain edge is remarkably graded even just after the implantation, so that maximum electric field is remarkably relaxed as compared with conventional transistor. And also the maximum point of lateral electric field at the drain edge is located apart from the main path of channel current and is located under the gate electrode. This tendency turned out to be promoted with increase of oblique angle and energy of implanted ions.

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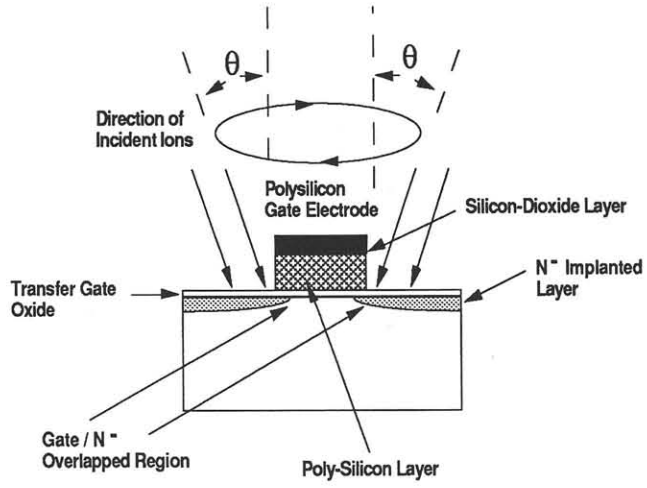

Fig.1 Schematic view of Oblique Rotating Ion Implantation

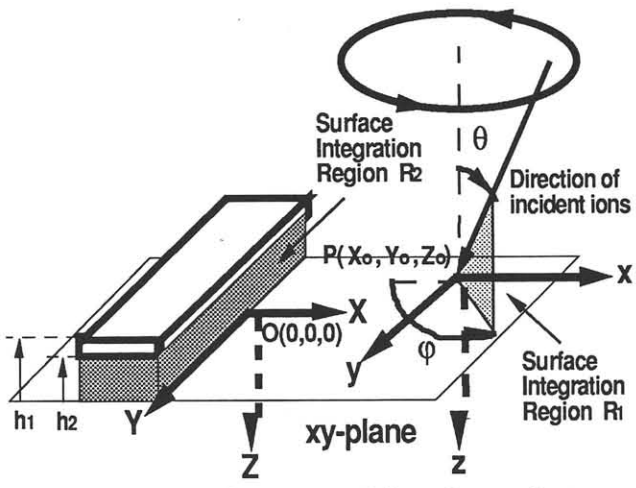

Fig.3 Setting-up of Coordinates System for deriving Theoretical Formula

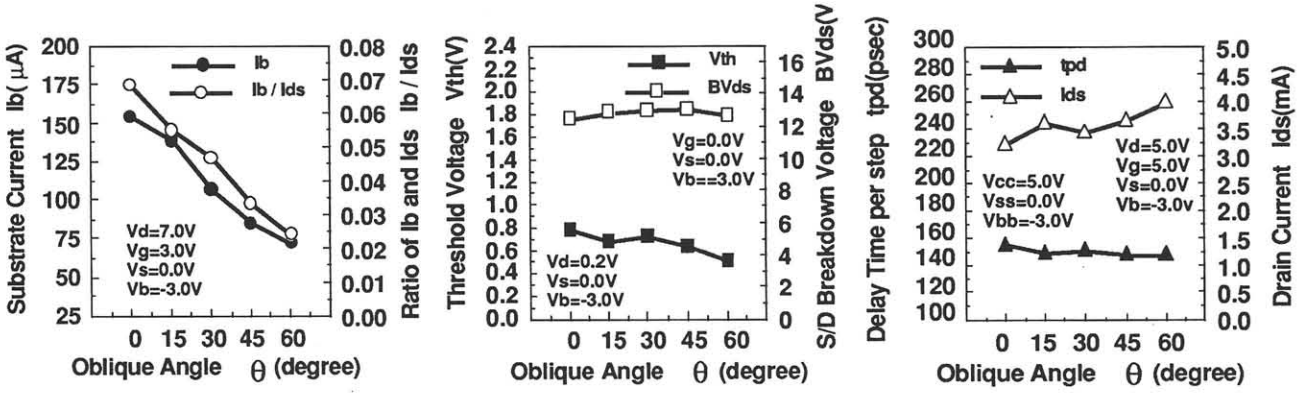

Fig.2 Dependence of Ib, Ib/Ids, Vth, BVds, tpd, and Ids on θ

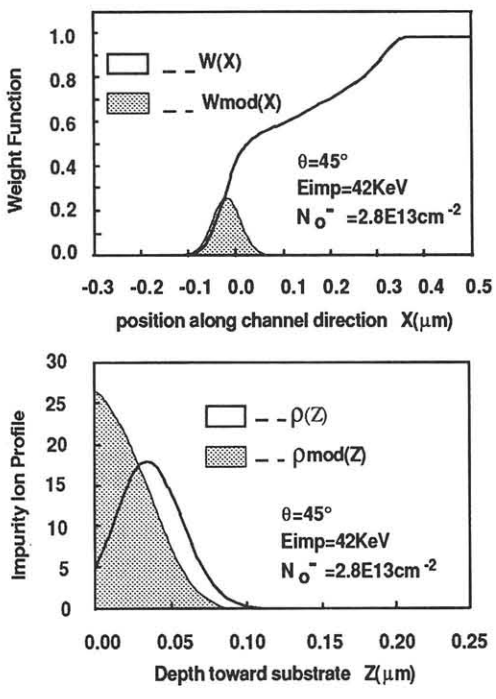

Fig.4 Numerical Calculation of W(X), Wmod(X), ρ(Z) and ρmod(Z)

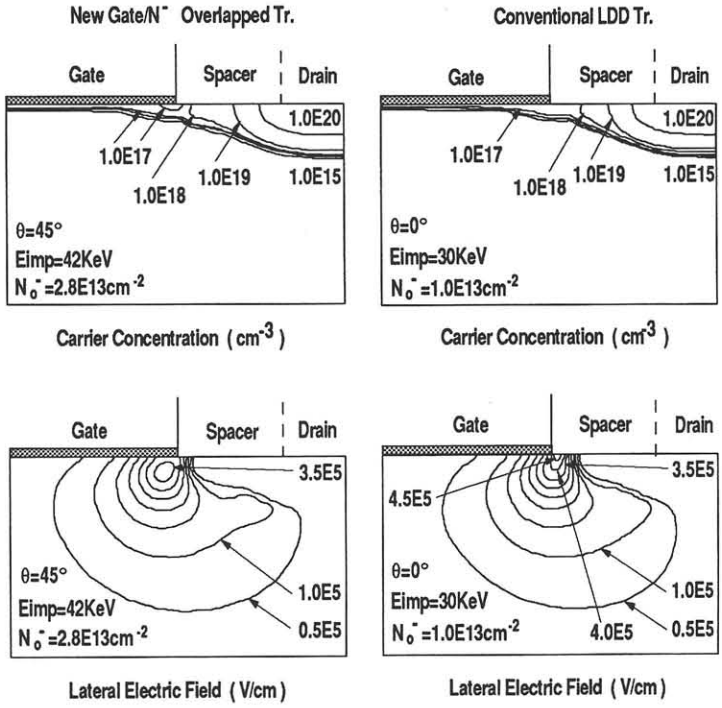

Fig.5 Simulation of Lateral Electric Field and Carrier Concentration