Extended Abstracts of the 21st Conference on Solid State Devices and Materials, Tokyo, 1989, pp. 481-484

S-D-7

High Reliability of Ultrathin Improved SiN on Poly Si

Shigeaki Ide, Hisakazu Miyatake, Hideo Komiya, and Masatoshi Ohshima
VLSI Development Laboratories IC Group
SHARP Corporation
Tenri City Nara 632 Japan

The ultrathin improved SiN film which was formed by removing top oxide from SiO_2/SiN stacked dielectric film on poly Si was investigated on the electrical properties. From these results, the ultrathin improved SiN(Top Oxide Removed SiN;T.O.R.SiN) revealed 3.8nm SiO_2 equivalent thickness and was superior to SiO_2/SiN on TDDB(Time Dependent Dielectric Breakdown). This T.O.R.SiN is hopeful as dielectric film for memory capacitor in DRAM more than 16M bits.

1.Introduction.

In dielectric film on poly Si for the memory capacitor of DRAM, SiO_2 has poor dielectric breakdown characteristics and, SiN is not desirable in its large leakage current. Recently, SiO_2/SiN films which make up for both deficiency of SiO_2 and of SiN are frequently investigated for the formation of the stacked type memory capacitor. Its thinnerization is attained to 5nm SiO_2 equivalent thickness.[1] However, in previous reports, the leakage current through the film is reduced[2] and TDDB characteristics are improved[3] by forming a thicker top oxide of the SiO_2/SiN film. But the increase of top oxide thickness goes against the thinnerization of the SiO_2/SiN film in order to increase the capacitance of memory devices.

In this paper, the results of investigation on T.O.R.SiN are discribed as compared with thin SiN films and the SiO_2/SiN films, and it is shown that T.O.R. SiN is the promising dielectric film for deep submicron DRAM.

2.Experimental

In order to evaluate the electrical properties of T.O.R.SiN, SiO_2/SiN film and SiN, MOS varactors were fabricated in the following procedures.

The Si substrate was N type <100> and 3~6Ωcm in resistivity. Plate electrode, a 450nm thick poly Si film was deposited on Si substrate by LPCVD and then the phosphorous doped with $POCl_3$ at 850℃ for 60minutes. A 8.5nm thick SiN film was formed under NH_3/SiH_2Cl_2 atmosphere in 770℃ by LPCVD on the poly Si. The SiO_2/SiN film was formed by thermal oxidation on SiN in steam ambient at 950℃ for 20 minutes. To fabricate the T.O.R.SiN, the top oxide of SiO_2/SiN film was removed by HF solution in diluted 0.49 wt%. The top electrode on these dielectric films was formed with phosphorous doped poly Si in a similar method as the plate electrode. The poly Si electrode area were 0.16~4.0mm^2. The thickneess of these dielectric films were estimated as SiO_2 equivalent thickness from the accumulation region of C-V curves, and examined by cross sectional TEM observation. These dielectric films were measured on I-V characteristics,

dielectric breakdown characteristics and TDDB.

3.Results and Discussion

3-1.Thickness of T.O.R.SiN

The SiO_2 equivalent thickness of SiN, SiO_2/SiN, and T.O.R.SiN is shown in Fig.1. The relative dielectric constant of SiN film was estimated to be 8.4 from C-V characteristics and TEM observation. A 3.8nm SiO_2 equivalent thickness of T.O.R.SiN was obtained by removing the top oxide of SiO_2/SiN, whose equivalent SiO_2 thickness was 5.2nm. Therefore, the top SiO_2 thickness should be 1.4nm and this thickness value is consistent with the value obtained from TEM observation in photo.1 (a),(b). Incidentally, from TEM about 1.0nm thick oxide was recognized between SiN and plate poly Si. This oxide might be natively grown before SiN deposition.

In memory capacitor for DRAMs using 3.8nm SiO_2 equivalent thickness of T.O.R.SiN, a capacitance of 8.9fF/μm^2 is obtained. This capacitance value is about 40% larger than the 5.2nm(=SiO_2) thick SiO_2/SiN film with 6.3fF/μm^2.

3-2. HF Tolerance of T.O.R.SiN

The relation between the diluted HF dipping time of SiO_2/SiN to remove the top oxide and the SiO_2 equivalent thickness is shown in Fig.2. The etch rate of top oxide of SiO_2/SiN is almost similar with the etch rate of thermally grown SiO_2 on single crystalline Si, with etch rate 3.0nm/min. After the top oxide is removed completely, the thickness of the T.O.R.SiN film is hardly reduced. The etch rate of T.O.R.SiN in diluted HF, 0.1nm/min, is less than that of SiN, 0.6nm/min. This fact indicates that T.O.R.SiN has excellent HF torelance and the thickness control of T.O.R.SiN is easy.

Fig.3 shows the defect density of T.O.R.SiN evaluated from the dielectric breakdown characteristics for various HF dipping time. The defect density of T.O.R.SiN is not degradated with the treatment of diluted HF, especially, even if long times for over etch off the top oxide are used.This fact indicates that the method of HF treatment to fabricate T.O.R.SiN is good enough to insure the electrical properties.

3-3.Leakage current in T.O.R.SiN

The leakage current of SiO_2/SiN film(=5.2nm SiO_2) is reduced to 1/5 compared with that of SiN film which have the Pool-Frenkel type conduction. Furthermore T.O.R.SiN shows just the same J-E characteristics as SiO_2/SiN in Fig.4. From these facts, the followings are infered. 1)the existance of the top oxide of SiO_2/SiN might not take part in J-E characteristics of SiO_2/SiN. 2)thermal oxidation on SiN causes the improvement of SiN which determines the J-E characteristics of SiO_2/SiN.

However, in the case of thick SiN film, if the top oxide thickness of SiO_2/SiN film is thicker than 3.0nm, the leakage current of SiO_2/SiN film is reduced in Pool-Frenkel conduction region. This result agrees with previous report[2]. Furthermore the J-E characteristics of T.O.R.SiN fabricated from the SiO_2/SiN using the thick SiN film are near to that of as-deposited SiN.

3-4.TDDB characteristics of T.O.R.SiN

TDDB characteristics of T.O.R.SiN were evaluated with the time to 50% failures on the constant voltage TDDB. these results are shown in Fig.5. From the relation of the time to 50% failures and the reciprocal of electric field, T.O.R.SiN has the best long-term reliability among these films.

In order to investigate the reason why T.O.R.SiN is better in TDDB than SiO_2/SiN film, leakage current variation from initial to dielectric breakdown in constant bias stresses were measured. These results are shown in Fig.6. T.O.R.SiN shows less leakage current variation than SiO_2/SiN. From these results, the interaction of conductive

carrier might be less to T.O.R.SiN than to SiO_2/SiN. It is considered that T.O.R.SiN might not have the interface such as SiO_2/SiN films, then the accumulated trap which cause dielectric breakdown is lesser in T.O.R.SiN than in SiO_2/SiN.

4.Summary

Thermal oxidation on ultrathin SiN causes the improvement of SiN on poly Si. This improved SiN, T.O.R.SiN presented 3.8nm SiO_2 equivalent thickness, and has small leakage current, in fabrication by using a 8.5nm thick SiN. Furtheremore T.O.R.SiN has higher reliability in TDDB than the SiO_2/SiN films. T.O.R.SiN is the promising dielectric film for memory capacitor of DRAMs with more than 16M bits.

5.Acknowledgement

The authors wish to thank Mr.A.Nakano for observation of TEM.

References

1)J.Yugami, T.Mine, S.Iijima, and A.Hiraiwa;Ext. Abst. 20th Conf. on Solid State Devices and Mat.(1988) p 173.

2)K.Kobayashi et al. Ext. Abst.(The 49th Spring Meeting, 1988) p.577.

3)K.Yoneda et al. Ext. Abst.(The 49th Spring Meeting, 1988) p.578.

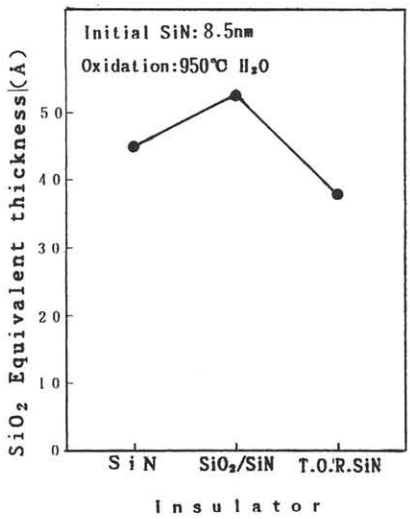
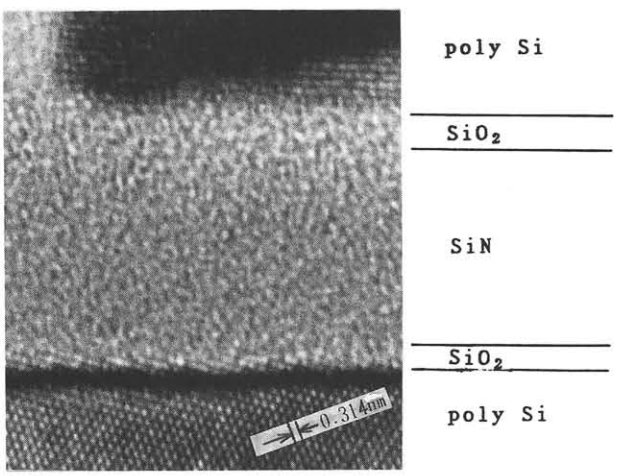
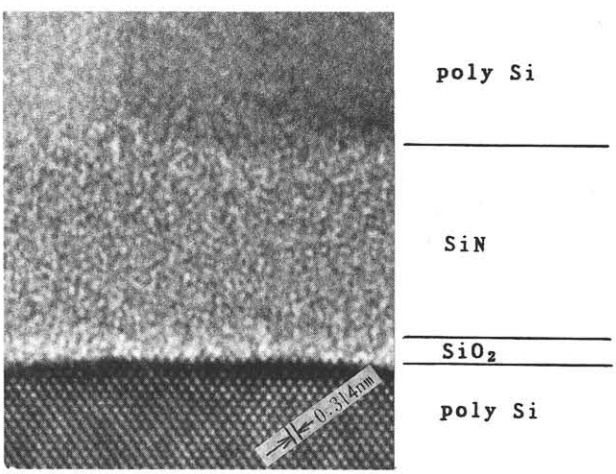


Fig.1 SiO_2 Equivalent thickness of various insulators.



(a) SiO_2/SiN stacked film.



(b) T.O.R.SiN.

Photo.1 TEM micrograph of the SiO_2/SiN stacked film and the T.O.R.SiN. (Cross section)

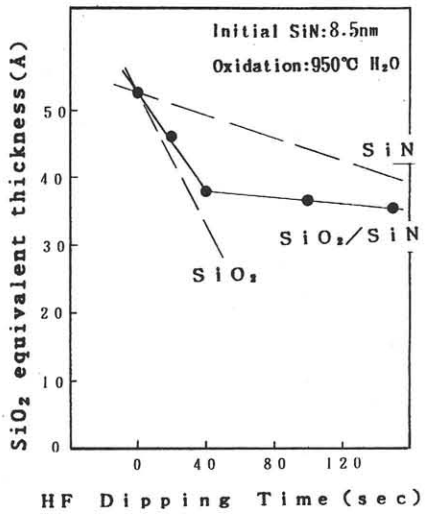


Fig.2 Relationship between SiO_2 equivalent thickness and HF dipping time.

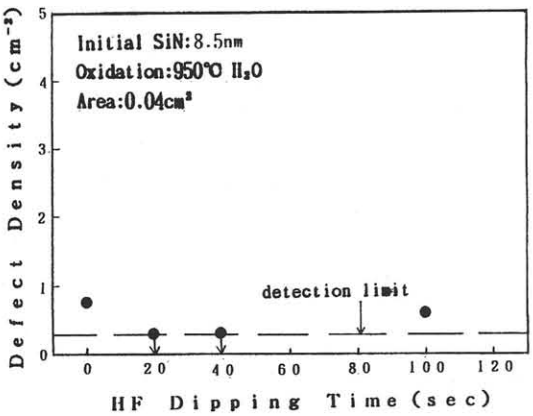


Fig.3 Defect density versus HF dipping time.

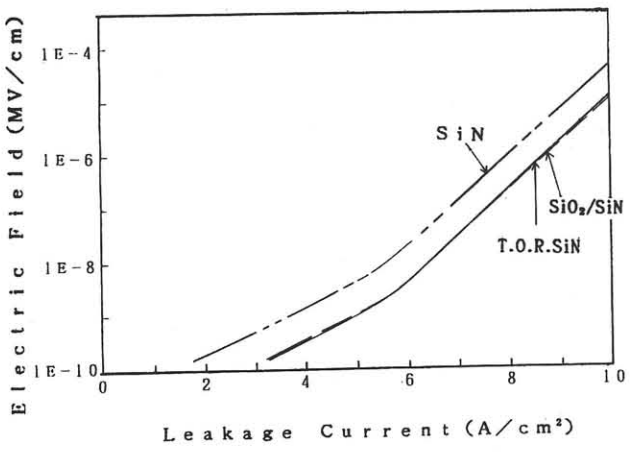


Fig.4 Leakage current characteristics of various insulators.

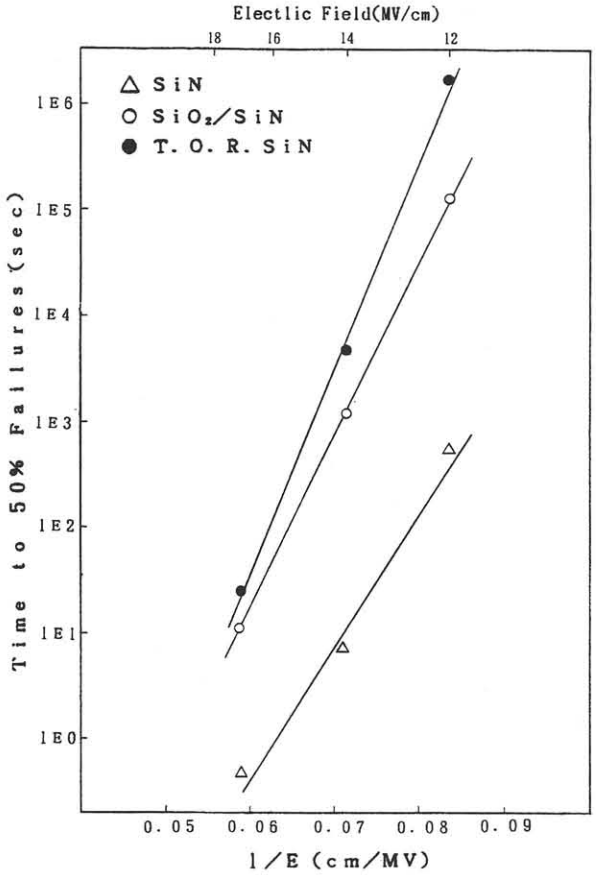


Fig.5 Time to 50% failures versus electric field.

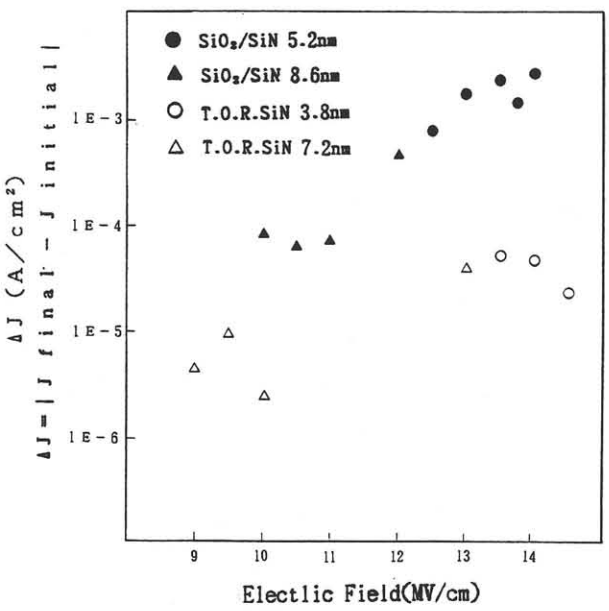


Fig.6 ΔJ versus Electric field.