Extended Abstracts of the 21st Conference on Solid State Devices and Materials, Tokyo, 1989, pp. 485-488

Conduction in Thin Nitride Films and Oxide/Nitride Films

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The conduction mechanisms in the silicon nitride film of 11 nm thick on the n^+ polysilicon has been investigated. The nitride was deposited using LPCVD method. At high fields the conduction current under positive gate bias can be separated into three current components, which are due to the two types of the Poole-Frenkel emission and the tunnel emission. The two types of Poole-Frenkel emission relate to the trap levels with the barrier height of 1.0 and 1.3 eV. The current transports under positive and negative gate biases are due to the same mechanisms. The current conduction at low fields has been also studied.

For thermally oxidized silicon nitride films, the conduction current at high fields under positive gate bias indicates a remarkable decreasing over the top-oxide thicktness of about 3 nm. The conduction current are reduced by the prevention of hole injection at the thick-top-oxide.

I. INTRODUCTION

Thermally oxidized silicon nitride films have attracted attention for capacitor dielectrics of submicron dynamic RAMs [1,2]. It is important to analyze the electrical properties and the conduction mechanisms to apply the oxide/nitride dielectrics to cell capacitors in dynamic RAMs.

The conduction mechanisms in silicon nitride have been investigated by several authors [3-8]. Sze discussed that the conduction current was due to three mechanisms, which were the Poole-Frenkel emission, the tunnel emission and the hopping of thermally excited electrons [3,4]. The charge carriers across SONOS structures were discussed by Liou and Chen. It was claimed that the conduction through the top-oxide and the nitride was dominated by hole flow under positive gate bias [8].

In this study, the charge-transport across the thin nitride film has been investigated. A dependence of the conduction current across the oxidized nitride film on the top-oxide thickness was also studied.

II. EXPERIMENTAL

The silicon nitride film of 11 nm thick was deposited on the n^+ polysilicon using LPCVD. Top-oxide films with various thicknesses were thermally grown on the nitride at 900 ℃. The upper-electrode was formed by phosphorus doped polysilicon. After aluminum metallization, all the samples were annealed at 450 ℃ in a hydrogen ambient.

The thicknesses of each dielectric layer were obtained from cross-sectional TEM observations and capacitance measurements. The oxide-equivalent-thicknesses (teff) of top-oxide/nitride/bottom-oxide multi-layer films were calculated from the capacitance using the relative dielectric constant of thermal oxide, 3.8. The teff was varied to range from 7.4 to 10.0 nm. The electric current-field (I versus E) characteristics were measured at the temperature range from -196 to 197 ℃.

III. RESULTS AND DISCUSSION

(a) Current-Field Characteristics

Raider et al. reported that the silicon nitride surface was rapidly oxidized at room temperature, even in air [9]. From the cross-sectional TEM observation of our sample, it is also found that there exists the top-oxide with a thickness of 1.0 nm on the non-oxidized nitride surface.

Figure 1 shows current density versus effective electric field (J versus Eeff) characteristics of the nitride under both positive and negative gate biases. The top-oxide thicknesses are 1.0, 2.7 and 4.1 nm, respectively. The effective electric field (Eeff) is obtained from the voltage across the dielectric films and the oxide-equivalent-thickness (teff). The current density at high fields (above about 6 MV/cm) is strongly dependent on the top-oxide thickness under positive gate bias. The slopes of J-Eeff curves at high fields under negative

gate bias are slightly changed as the top-oxide thickness increases. It is also noted that the slopes at low fields of the J-Eeff curves are small as compared with those at high fields under both positive and negative gate biases. The current conduction at low and high fields is expected to be due to different mechanisms.

(b) Conduction in Thin Nitride Film

Figure 2 shows the current density J versus 1/T plots for the thin-top-oxide/nitride/bottom-oxide structure with the teff of 7.4 nm. It is found that the J versus 1/T plots can be separated into three straight lines. The conduction current at high fields under positive gate bias is constructed by three current components, J1, J2 and J3, as shown in Fig.3. The current component J2 is independent of temperature. As same as the discussion by Sze [3,4], it is considered that the J2 is due to the tunnel emission.

The current component J3, which is dominant at moderate temperatures (around room temperature), is dependent on temperature. The thermal activation energy Ua obtained from the slope of the J3 in Fig.3 is 0.13 eV. The conduction current at high fields and room temperature exponentially increases as the electric field linearly increasing, as shown in Fig.1. On the basis of these two facts, it is considered that the J3 is defined by the Poole-Frenkel emission process.

Figure 4 shows a characteristic of current density versus square root of the electric field across the nitride film ($\sqrt{En}$) for the thin-top-oxide/nitride/bottom-oxide structure. The En is the electric field across the nitride. The Poole-Frenkel current is given by Eq. (1) :

$$J \propto En \cdot \exp\{-q[\phi_i - (qEn/\pi\varepsilon_0\varepsilon_n)^{\frac{1}{2}}]/kT\} \qquad (1),$$

where ϕ_i is the barrier height of trap level in the nitride, ε_0 the dielectric constant of free space, ε_n the dynamic dielectric constant in the nitride and k the Boltzmann constant. LogJ at high fields shows a linear relation to $\sqrt{En}$ as shown in Fig.4. The ε_n is 4.3, calculated from Eq.(1) and the slope of the logJ versus $\sqrt{En}$ plot. This value is consistent with the dielectric constant, 4, in the optical range and the static dielectric constant, 6.3. The barrier height of trap levels related to the Poole-Frenkel emission is obtained to be 1.0 eV.

The current component J1 gives the thermal activation energy of 0.46 eV, obtained from the slope in Fig.3. It has been discussed that the conduction at high fields and high temperatures was due to the Poole-Frenkel emission. If the J1 is due to the Poole-Frenkel emission, the barrier height ϕ_1 calculated from the thermal activation energy and Eq.(1) is found to be 1.3 eV, which agrees with the value obtained by Sze [3]. It is suggested that the J1 is also based on the Poole-Frenkel emission.

At low fields under positive gate bias the conduction current is separated into two current components, j3 and J4. The j3, which is dominant at high temperatures, is substantially dependent on temperature and the thermal activation energy, 0.40 eV, is obtained from Fig.3. Assumed that the j3 is due to the Poole-Frenkel emission, the barrier height is calculated to be 1.0 eV, which agrees with the value of the J3. Thus the j3 is defined as the low-field-component of the J3. The J4, which is dominant at moderate and low temperatures, is weakly dependent on temperature. The thermal activation energy is found to be about 0.01 eV.

For negative gate bias in Fig.2, since the current density is independent of temperature at high fields and low temperatures, the dominant current component is originated from the tunnel emission as well as the J2 under positive gate bias. The conduction current at high fields above room temperature depends on temperature and can be separated into two current components. The thermal activation energies of these two current components are calcurated to be 0.43 and 0.13 eV and those are similar to the values obtained from the current components, J1 and J3, under positive gate bias.

Therefore it is concluded that the current conductions under positive and negative gate biases are due to the same mechanisms, i.e. two kinds of the Poole-Frenkel emission and the tunnel emission.

(c) Dependence on Top-oxide Thickness

Figures 5 (a) and (b) show the dependence of the current density at high fields (±9 MV/cm) on the top-oxide thickness. It is found that the current density under positive gate bias indicates a remarkable decrease at about 3 nm. The current density under negative gate bias is slightly dependent on the top-oxide thickness.

Figure 6 shows the current density versus 1/T plots for the thick-top-oxide/nitride/bottom-oxide structure with the teff of 10.0 nm. Under positive gate bias, the conduction current at high fields can be separated into three current components. It is noted that the current components J1, J2 and J3 under positive

gate bias decrease together as the top-oxide thickness increases. The current reductions caused by the thick-top-oxide are explained as follows : The J1 and J3 are due to the Poole-Frenkel emission of holes in the nitride. The hole injection from upper-electrode to the nitride is prevented by the thick-top-oxide. The J2 is controlled by hole tunneling from the upper-electrode. The hole tunneling is blocked by the thick-top-oxide. So the current components, J1, J2 and J3, indicate the remarkable reductions under positive gate bias.

At high fields under negative gate bias in the thick-top-oxide/nitride/bottom-oxide structure in Fig.6, the current density versus 1/T plots essentially behave in the same manner with the case of the thin-top-oxide/nitride/bottom-oxide structure in Fig.3. The conduction at low temperatures is considered to be governed by the tunnel emission process. The thermal activation energies obtained from the current components at high and moderate temperature range are 0.40 and 0.14 eV, which are similar to the values obtained from the J1 and J3 in the thin-top-oxide/nitride/bottom-oxide structure. Therefore it is suggested that the current conduction under negative gate bias in the thick-top-oxide/nitride/bottom-oxide structure is essentially dominated by the same mechanisms as the current conduction under positive gate bias in the thin-top-oxide/nitride/bottom-oxide structure.

IV. CONCLUSIONS

(1) The conduction mechanisms in the silicon nitride film of 11 nm thick on the n^+ polysilicon was investigated. The nitride film was deposited using LPCVD method. At high fields the conduction current under positive gate bias can be separated into three current components and those are due to the two types of the Poole-Frenkel emission and the tunnel emission. The two types of Poole-Frenkel emission relate to the trap levels with the barrier height of 1.0 and 1.3eV. The current conduction under positive and negative gate biases is due to the same mechanisms. At low fields the conduction current is separated into two current components. One is due to the Poole-Frenkel emission. Another is weakly dependent on temperature and indicates the thermal activation energy of 0.01 eV.

(2) For thermally oxidized silicon nitride the conduction current at high fields under positive gate bias indicates a remarkable decrease with the top-oxide thickness increase. The current reduction is caused by the thick-top-oxide, which controls hole injection and hole tunneling from anode. The current transport at high fields under negative gate bias is essentially dominated by the same mechanisms as the current conduction under positive gate bias in the thin-top-oxide/nitride/bottom-oxide structure.

The authors would like to thank Dr. H. Koyama, Mr. J. Mitsuhashi, Mr. Y. Mashiko, Mr. N. Yutani and Dr. T. Kato for their valuable suggestions and help in the electrical measurement.

REFERENCES

1) Y. Ohji, T. Kusaka, I. Yoshida, A. Hirata, K. Yagi, K. Mukai and O. Kasahara : *Proc. Int. Reliability Phys. Sympo.* (1987) p.55.
2) Y. Ohno, T. Kaneoka, I. Ogoh, J. Mitsuhashi, M. Hirayama and T. Kato : *Sympo. VLSI Tech. Dig.* (1988) p.35.
3) S. M. Sze : J. Appl. Phys. **38** (1967) 2951.
4) S. M. Sze : *Physics of Semiconductor Devices* (John Wiley & Sons, New York, 1981) p.402.
5) Z. A. Weinberg and R. A. Pollak : Appl. Phys. Lett. **27** (1975) 254.
6) P. C. Arnett and Z. A. Weinberg : IEEE Trans. Electron Devices **ED-25** (1978) 1014.
7) D. K. Schroder and M. H. White : IEEE Trans. Electron Devices **ED-26** (1979) 899.
8) F. T. Liou and S. Chen : IEEE Trans. Electron Devices **ED-31** (1984) 1736.
9) S. I. Raider, R. Flitsch, J. A. Aboaf and W. A. Pliskin : J. Electrochem. Soc. **123** (1976) 560.

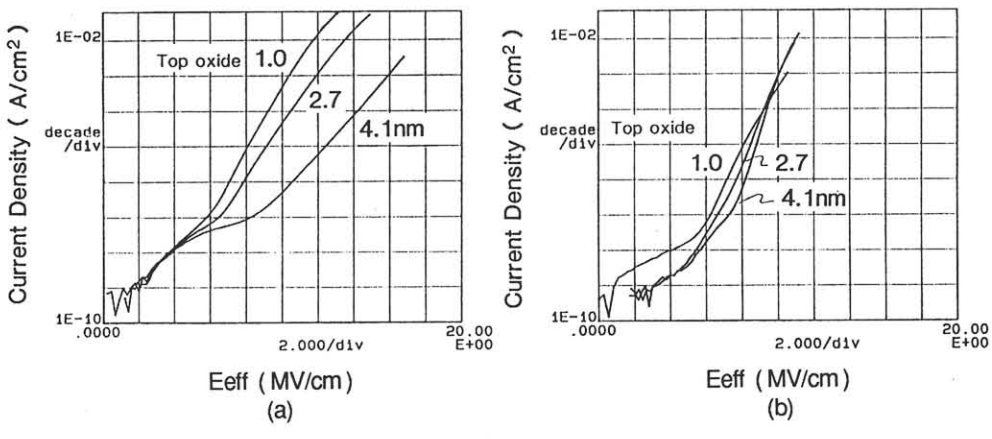

Fig.1 Current density vs. Eeff. (a) Positive gate bias (b) Negative gate bias. The Eeff is obtained from the gate voltage and the oxide-equivalent-thickness.

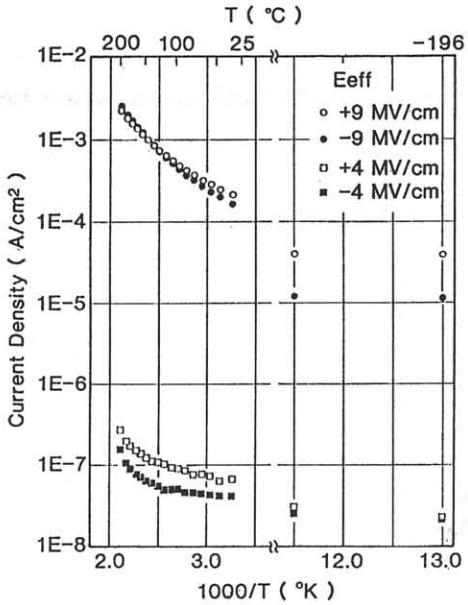

Fig.2 Current density vs. 1/T plots under positive and negative gate biases for thin-top-oxide(1.0nm)/nitride/bottom-oxide structure.

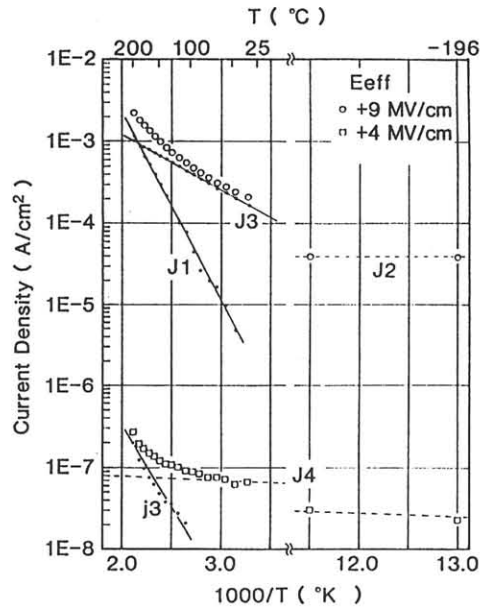

Fig.3 Current components under positive gate bias. The conduction current can be separated into three components, J1, J2 and J3.

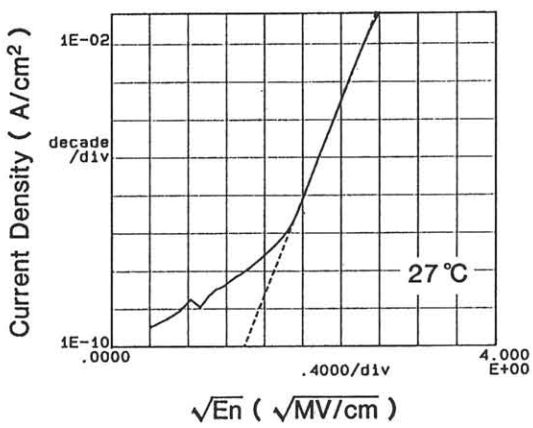

Fig.4 Current density vs. √En at room temperature. The En is electric field across the nitride.

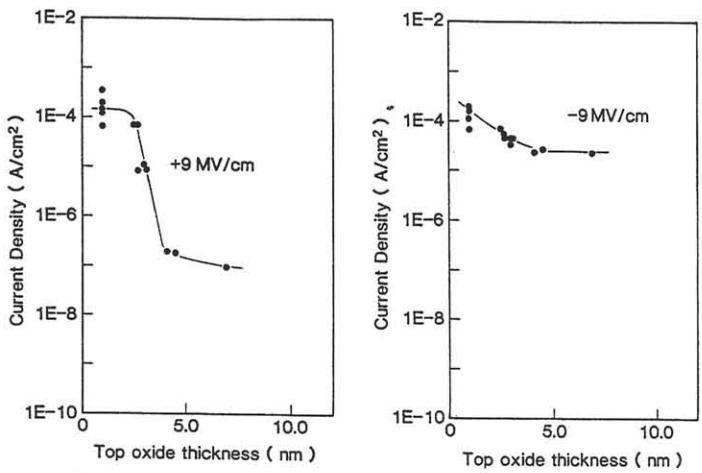

Fig.5 Current density vs. top-oxide thickness. (a) +9 MV/cm (b) -9MV/cm.

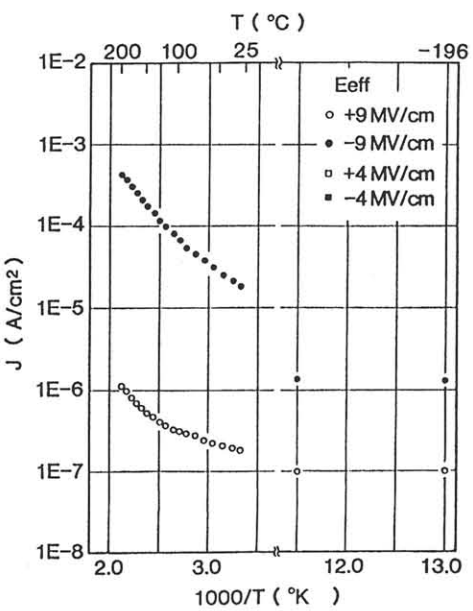

Fig.6 Current density vs. 1/T plots for thick-top-oxide(4.1nm)/nitride/bottom-oxide structure under positive and negative gate biases.