Perspectives on ULSI MOS Devices and Advances towards Si Quantum Devices

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Perspectives and limitations on ULSI MOS FETs are reviewed and discussed from the viewpoint of performance and reliability. Based on these considerations, the importance of quantum devices, in particular, Si quantum devices" in the region less than ~ 0.1 \( \mu m \), is emphasized. In the deep submicron region (0.1 - 0.3 \( \mu m \)), the threshold voltage (Vth) has to be scaled down to maintain high performance with the power supply voltage down-scaling. This demands a new technique - "substrate engineering" - to achieve both Vth-scaling and suppressed Vth-lowering simultaneously. However, after these deep submicron ULSIs are highly diversified to system applications, quantum phenomena which emerge from ~ 0.1 \( \mu m \) region even in Si should/can be used as a device operating principle, rather than warning for device reliability.

I. INTRODUCTION

"ULSI revolution" marking a new epoch in the electronic industry has made remarkable progress to such an extent that 10 \(^7\) - 10 \(^9\) transistors are fabricated on a single chip. For instance, current ULSI microfabrication technologies are being pushed to the extremes by the DRAM community, thereby expediting research on 64 Mbit DRAMs using a 0.3 \( \mu m \) design rule. Giga-bit DRAMs and sophisticated ULSI processors using ~ 0.1 \( \mu m \) MOSFETs could possibly appear in the latter half of the 1980s. Also, recently, a very high speed of 10 psec/gate has been achieved at 77 K in the ring oscillator level by the IBM group[1]. This speed is comparable to those of conventional quantum devices such as HEMT[2], JJ[3], and STC [4], as shown in Fig. 1.

From a manufacturing standpoint, process and device technologies in the deep submicron region (0.1-0.3 \( \mu m \)) are, however, approaching practical limits and thus coincident achievement of high performance and high reliability becomes increasingly difficult. For the scaled MOSFET (ULSI building element) in particular, the Vth-scaling required by power supply voltage reduction and associated short-channel effects such as punch-through demand attention. In the submicron era (0.5 - 1.0 \( \mu m \)), on the other hand, high field hot-carrier effects were the most important problems. In addition, the region less than 0.1 \( \mu m \) is still a grey zone and is entering the quantum region. Such a trend requires a deeper physical insight into a new scaling law and new device operation.

In this paper, the state-of-the-art and future perspective of MOS devices and advances toward Si quantum devices are reviewed and discussed from the viewpoint of: 1) new problems in the deep submicron MOSFETs, 2) device structures for use with low supply voltage, 3) Bi-CMOS strategy for ULSI system application, and 4) Si quantum effects and its applications in the region < 0.1 \( \mu m \).

II. PERSPECTIVES ON SCALED MOSFETS

The most significant problem in MOS devices scaled down to 0.5 \( \mu m \) has been a hot-carrier effect (high field effect) caused by a non-scaling approach of power supply voltage. To avoid the hot-carrier device degradation,
several kinds of hot-carrier resistant device structures such as DDD[5] and LDD[6] (drain engineering) have been proposed so far. Furthermore, recently, much attention is paid to the GOLD [7-8] structure with high reliability and high transconductance, which makes a good use of gate-to-drain overlapped effect.

However, in the deep submicron region, the power supply voltage reduction is inevitable from the point of view of power consumption, as well as reliability. Therefore, device structures, and device operation, and circuit design to obtain high speed in the low supply voltage (1.5-3 V)[9-10] become more important from now on.

A. Performance Limitation

Figure 2 shows the delay time under the ring oscillator condition of FL=FO=1 as a function of LEFF. The power supply voltage was determined by hot-carrier breakdown voltage for each LEFF. In the case of non Vth-scaling (Vth=0.55 V at 300 K and Vth=0.25 V at 77 K), the minimum channel length which provides the minimum delay time (performance limits) is ~ 0.1 µm at R.T. and ~ 0.03 µm at 77 K, respectively[11]. These values are consistent with those mentioned above[1]. On the other hand, if the threshold voltage can be scaled down in proportion to the supply voltage scaling, the minimum channel length would extend to ~ 0.05 µm at R. T.

However, the Vth-scaling requires a decreased impurity concentration at the channel, unlike a conventional scaling law[12], which degrades subthreshold characteristics (Vth-lowering). Therefore, a new device structure to achieve both Vth-scaling and short-channel resistance simultaneously would be indispensable.

B. Vth-Scaling Technology[13]

The empirical relationship between the possible minimum channel length, LMIN, and a parameter (NS+NJ) 2 is shown in Fig. 3. NS and NJ are Si surface and substrate doping doses at source-drain junction depth XJ, respectively. (NS+NJ) 2 implies the average doping level at 0.05 ~ 0.1 µm depth, calculated by process simulator. It is found from Fig. 4(a) that

\[ L_{\text{MIN}} \propto \left( \frac{N_S + N_J}{2} \right)^{1/3} \]  

is valid over wide ranges of Tox, XJ, and substrate doping profile. The dotted line is an expression of two-dimensional simulation results, analogous to Eq. (1).

One of the characteristics of Fig. 4 is that Eq. (1) is independent of Vth at any given Tox, XJ, and substrate doping. As a result, a general guideline for scaling down Vth without punchthrough, reducing NS and increasing (NS+NJ) 2 at 0.05~0.1 µm depth, can be obtained. This approach leads to thin film SOI structures[14].

III. MOSFET/BIPOLAR IN BI-CMOS CIRCUITS

The Bi-CMOS is changing from a simple compromise between bipolar and CMOS to a strategic device conforming to diversified ASICS and new system architectures such as RISC. Namely, this technology will allow the construction of future ULSIs by compensating for demerits of both devices. However, there are two significant problems in scaled Bi-CMOS devices: ① degradation of circuit performance due to supply voltage reduction and ② a setting of performance balance between bipolar and CMOS for various ULSIs.

A. Power Supply Voltage vs. MOS Structures[15]

The power supply voltage reduction causes a fatal speed degradation in Bi-CMOS circuits. This is because an effective voltage applied to the MOSFET is reduced due to a built-in voltage (Vbe ~ 0.7 V) in a conventional totem-Pole type circuit as shown in Fig. 4, leading to a more severe channel current decrease with a reduced supply voltage. To overcome this problem, the following two approaches are possible: ① such a hot-carrier resistant device structure as GOLD usable at a 5 V
supply voltage and new circuit concept in the low supply.

Figure 5 shows supply voltage scaling effect on the Bi-CMOS drivability with device structures as a parameter. Although the delay times of the CMOS gate show almost the same dependence, BiCMOS gate is strongly dependent on the MOS device structure or Vcc due to the Vbe effect. Thus, it is found that a hot-carrier resistant structure GOLD is a candidate for high-speed logic application of scaled BiCMOS.

IV. SI QUANTUM DEVICES

A. Quantum Effects

As device dimensions (< 0.1 μm) become comparable to electron wave length (De Blois wave length), quantum phenomena emerge even in Si. Research on quantum effects in Si has, in the first stage, begun for the purpose of discovering new phenomena related to ULSI reliability, rather than proposing new quantum devices. These are playing a role of "warning" to future ULSIs. The following phenomena, as shown in Table 1, have been reported as main quantum effects (size effects) in Si: ① impurity fluctuation[16] ⇒ Vth scattering, ② single electron trapping [17] ⇒ channel current scattering, ③ velocity overshoot[18] ⇒ channel current increase (1.4 times larger than expected by a simple scaling), and ④ transconductance abnormal in one-dimensional electron system[19] ⇒ Gm oscillation.

B. Quantum Devices

Although all phenomena except velocity overshoot are found to be related to reliability, these effects may trigger new quantum devices. As a cause of ④, universal conductance fluctuations or one-dimensional sub-bands in the narrow inversion layers is considered. Figure 6 demonstrates regular Gm oscillation measured in a novel twofold gate structure. The first gate is used to form a channel in an inversion layer and the second gate controls the channel width. It is obvious that a cycle period of Gm oscillation becomes longer with a decreased channel width. This fact implies that one-dimensional quantum energy levels in the inversion layer are formed. This quantum phenomenon can be used to construct a type of quantum interference device. In addition, the single electron transistor, which makes a good use of single electron trapping into gate oxide, has already been proposed[20].

Since the De Blois wave length in Si is smaller than that in GaAs, it seems to be more difficult to construct Si quantum devices. However, considering high-quality Si crystal and advanced Si ULSI production technologies, if Si quantum ULSIs are realized, the impact to electronic industry will be remarkable and GSI (Giga Scale Integration) revolution will newly come into existence. Therefore, to achieve such a marked progress, device innovation is strongly required.

V. CONCLUSIONS

Perspectives on the deep submicron MOSFETs and the necessity of Si quantum devices in the region < 0.1 μm were discussed. By using the Vth-scaling method ("substrate-engineering"), the limitation of scaled MOSFETs will extend to 0.05 μm even at 300 K. Moreover, several Si quantum phenomena emerge from the region < 0.1 μm. Perhaps, the giga-bit memories will be realized using ~ 0.1 μm MOS devices. However, some breakthrough beyond a "0.1 μm wall" is required, and in that case, it would be essential to understand a deeper physical meaning of Si quantum phenomena and to investigate its applications.

Reference
[13] R. Izaya et al., to be published in the 21st SSD&M.

Fig. 1 Delay time vs. power dissipation

Fig. 2 Gate length vs. delay time relation

Fig. 3 Possible minimum channel length

Fig. 4 Typical BiCMOS circuit

Fig. 5 Delay time vs. output capacitance in both Bi-CMOS and CMOS.

Fig. 6 gm oscillation due to one-dimensional quantum level in the inversion layer

Table 1 ULSI reliability problems