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Impact of VLSI Technology on Power Devices

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This paper evaluates the improvement in performance of power devices by the application of VLSI technology. It is demonstrated that the specific on-resistance of power MOSFETs can be reduced by a factor of 2 by utilization of finer design rules, silicided contacts, and trench gates. These technologies are also shown to be important to improving the characteristics of MOS-Bipolar devices, such as IGBTs and DMTs.

INTRODUCTION

For many decades after the invention of the basic bipolar devices (transistors and thyristors), power semiconductor technology and integrated circuit technology have taken divergent roads. The main reason for this has been the need to fabricate deep diffused junctions that can withstand high blocking voltages in power devices. In addition, the manufacturing of bipolar devices has been done using large design rules, with specifications given to mil units rather than in microns as in the case of integrated circuits, in order to reduce fabrication cost.

This picture changed in the 1970's with the introductions of power MOSFETs. For these devices, it is essential to utilize the same stringent design rules and cleanliness that is commonly used for integrated circuits. Modern power MOSFETS rely upon the paralleling of over 100,000 individual transistor cells to derive a high current handling capability. The resulting device can be viewed as a single transistor with a channel length of about 1 micron and a channel width of over 10 meters, i.e. a channel aspect ratio of over 10 million. Consequently, the technology for the fabrication of such chips is just as demanding as a memory chip, with the additional requirement that a short in any single cell makes the entire chip defective. Further, the device must be designed to support high voltages and operate at relatively high temperatures due to the power dissipation arising from self-heating during operation. From these facts, it becomes quite clear that the application of VLSI technology to these devices will be of importance in improving their performance.

POWER DMOSFET STRUCTURE AND FABRICATION

A cross-sectional view of the basic DMOSFET structure is shown in Fig. 1 and a typical square cell topology is illustrated in Fig. 2 with the important masking levels that dictate its size. The operation of the DMOSFET has been described in detail in reference[1)]. The device supports voltage across the P-base to N-drift region junction with a depletion layer extending into both regions. In order to avoid breakdown due to reach-through, it becomes necessary to have a channel length of about 1 micron. A positive gate bias is used to turn-on the device by the formation of an inversion layer at the surface of the P-base region under the gate electrode. The on-state current flows by electron transport from the N^+ source region, through the n-type inversion channel, into the drift region.

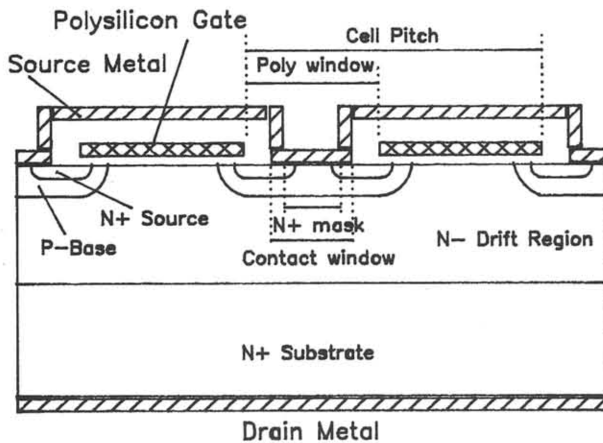

Fig.1 DMOSFET structure

The major contributors to the internal resistance to current flow have usually been identified to be (a) the channel, (b) the JFET region, where the drift region comes to the surface between the P-base regions, and (c) the drift region[2-5]. However, in an optimized 50 volt power MOSFET, the contact resistance to the N^+ source region becomes significant because the contact area is only a small percentage of the active area.

The fabrication of the power DMOSFET cell structure begins by the definition of the polysilicon gate pattern on the gate oxide. The P-base is implanted through the polysilicon window. The photoresist implant mask (N^+ mask) is then used to define the edges of the N^+ source region insider the polysilicon window, its outside edges being defined by the polysilicon. A low temperature glass is deposited and a contact window is then opened for connection to the source and base regions. The process requires two critical alignments which impact device performance and the size of the polysilicon window is determined by the lithographic tolerances. It will be shown in this paper that the use of VLSI technology to reduce the polysilicon window size results in improvements in the on-resistance of the power DMOSFET.

OPTIMIZATION OF DMOSFET DESIGN

Simulations of the specific on-resistance of DMOSFETs were done for the state-of-the-art (SOTA) DMOSFET and the VLSI based DMOSFET using the dimensions given in Fig. 2 for the case of different cell pitches

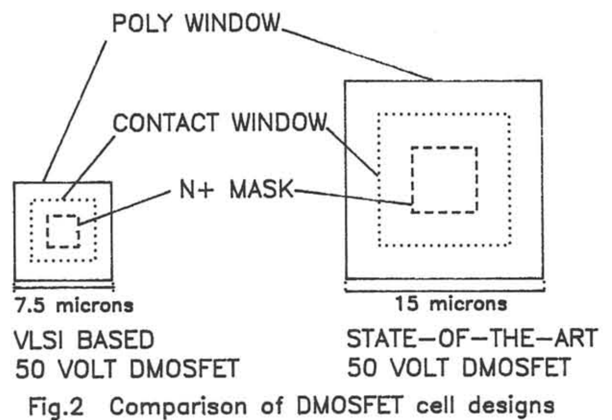

Fig.2 Comparison of DMOSFET cell designs

keeping the polysilicon window size fixed. The gate oxide thickness used was 1000 Å for the SOTA case and 500 Å for the VLSI case. The specific contact resistance for the SOTA devices was chosen as 1×10^{-5} ohm—cm^2 based upon aluminum metallization and that for the VLSI devices was 1×10^{-6} ohm—cm^2 based upon silicides. The results, shown in Fig. 3, demonstrate that a reduction in the specific on-resistance by a factor of 2 can be expected. This is consistent with experimental value recently reported in the literature[6-7].

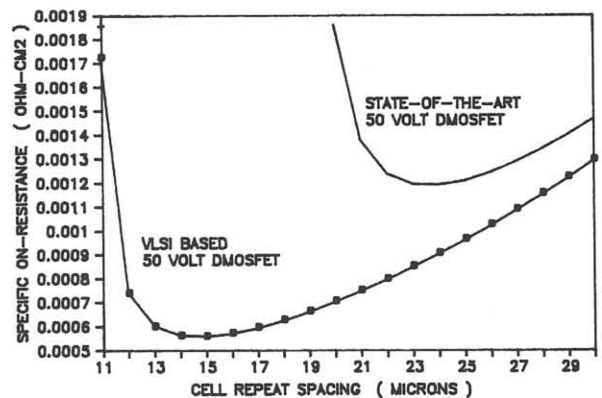

Fig.3 Impact of VLSI technology on 50V DMOSFET

IMPACT OF SOURCE CONTACT RESISTANCE

The process of scaling down the polysilicon window using VLSI lithography causes a reduction of the source contact area. As a consequence, the VLSI based devices become more sensitive to the magnitude of the specific resistance of the source contact metal. This is illustrated in Fig. 4, where the percent contribution of the source contact resistance to the total specific on-resistance of the MOSFET is plotted as a function of

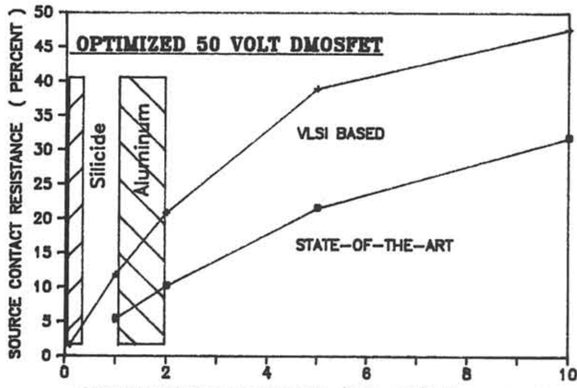

Fig.4 Impact of source contact resistance

the specific contact resistance of the source metal. Typical values of the specific contact resistance obtained using aluminum and silicides are indicated by the cross-hatched regions. From this illustration, it can be concluded that, although aluminum may be acceptable for SOTA DMOSFETs, its contact resistance is too high for the VLSI based DMOSFETs. The use of silicide technology is mandatory to obtaining the full benefits resulting from scaling the polysilicon window using VLSI lithography.

IMPACT OF GATE OXIDE THICKNESS

The SOTA DMOSFETs are fabricated using 1000 Å gate oxides. A reduction in the gate oxide thickness produces a significant decrease in the specific on-resistance, as shown in Fig. 5, by the results of simulations done on the VLSI DMOSFETs. As the oxide thickness is reduced, the channel resistance decreases. A reduction in the specific on-resistance by a factor of 2

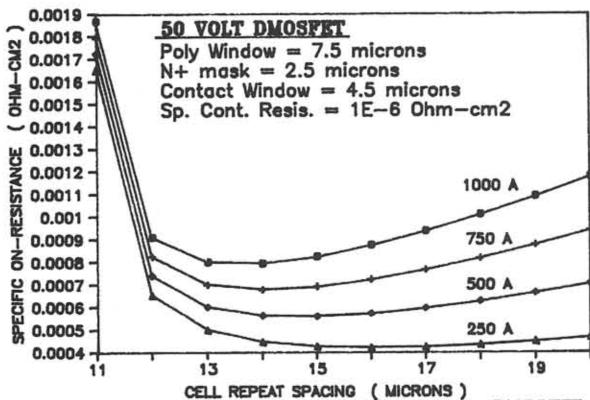

Fig.5 Impact of gate oxide thickness on DMOSFET

is projected by going from a gate oxide thickness of 1000 Å to 250 Å.

It is not well recognized that a reduction of the gate oxide thickness can improve other MOSFET characteristics. When the gate oxide thickness is reduced by a factor of 2, it is necessary to increase the peak P-base doping by a factor of 4 in order to maintain a constant threshold voltage. This greatly reduces the resistance of the P-base region which results in improvement in the dV/dt capability and the ruggedness of the DMOSFET[1].

TRENCH GATE TECHNOLOGY

Another VLSI technology that offers significant performance advantages for power MOSFETs is the fabrication of trench gate regions[8-9]. A cross-section of this device is shown in Fig. 6, with an indication of the current flow path in the drift region (cross hatched). It should be noted that almost all of the drift region is fully utilized for current transport, which minimizes the drift region resistance. By using a self-aligned process, the cell pitch can be made very small. The resulting high channel density allows reduction of the channel resistance. It has been experimentally demonstrated that, even with 3 micron design rules, a specific on-resistance of 0.4 milli-ohm cm^2 can be obtained for a 50 volt device[10-11].

An important consideration for the UMOSFET is the impact of the inversion layer mobility upon the channel resistance, because it has been reported that the reactive ion etching used to fabricate the trench gate regions produces surface damage, which is know to the cause degradation of the mobility[12]. The results of

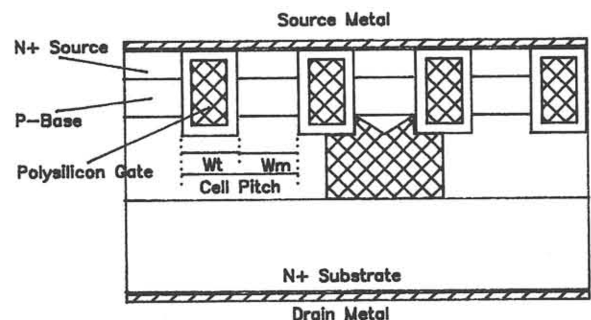

Fig.6 UMOSFET structure

simulations done on the impact of inversion layer mobility upon the specific on-resistance of UMOSFETs are provided in Fig. 7. For a cell repeat spacing of 6 microns, a reduction of the mobility from 500 to 100 $cm^2/v.s.$ produces an increase in specific on-resistance to values larger than those for the VLSI base DMOSFETs. It is necessary to examine methods to consistently obtain high mobility in trench gate structures before the improvements possible with the UMOSFET structure can be fully utilized.

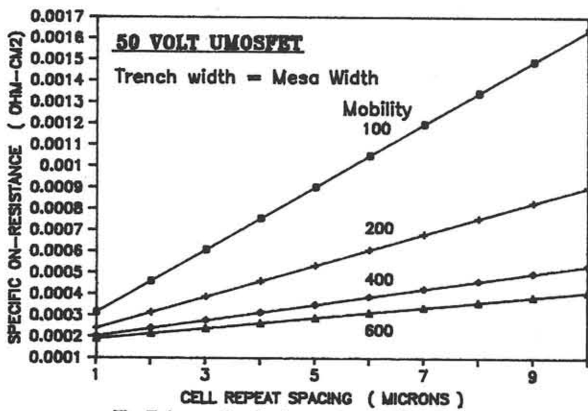

Fig.7 Impact of channel mobility on UMOSFET

IMPACT OF VLSI TECHNOLOGY ON MOS-BIPOLAR DEVICES

The trench gate technology described above in the context of the UMOSFET has applications for MOS-Bipolar devices. It has been shown that IGBTs made using trench gate structures have significantly better on-state characteristics than those made with the DMOS structure because of the increase in channel density[13]. In addition, these devices have high latching current densities and shorter switching times. The trench gate structures are particularly attractive for IGBTs with short switching times because the channel current component is larger of these devices.

The trench gate technology can also be utilized to create new MOS-Bipolar device structures, such as the depletion mode thyristor (DMT)[14]. In this case, the trench gate region is used to interrupt current flow within the two coupled transistors that form a latched-up thyristor in the on-state. Devices have been fabricated with 500 volt forward blocking capability with a forward drop of 1 volt at a on-state current density of over 200 amperes per cm^2. It has been found that current densities over 2000 amperes per cm^2 could be turned-off with a gate bias of 15 volts.

CONCLUSIONS

In this paper, it has been demonstrated that the application of VLSI technology can significantly reduce the specific on-resistance of power MOSFETs. In addition to the use of VLSI lithography, the utilization of silicided contact, thinner gate oxide, and trench gate technologies can improve power MOSFET performance. The historical trend in improving the specific on-resistance of power MOSFETs is indicated in Fig. 8. On this chart, the implementation of VLSI technology has been responsible for a reduction of the specific on-resistance below 1 milli-ohm cm^2. An important point to note from this figure is that the devices are now approaching the theoretical limit for silicon. Further improvements in power MOSFET performance will require investigation into other semiconductor materials, such as silicon carbide[15].

In addition, VLSI technology can play a role in improving the performance of MOS-Bipolar devices, such as IGBTs which are used for high voltage system applications. With the utilization of VLSI technology for all power devices will closely resemble those for integrated circuits, enabling the development of smart power chips for a large variety of system applications.

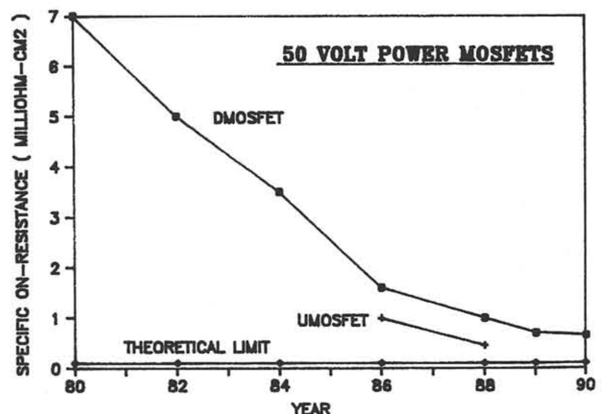

Fig.8 Progress in power MOSFET technology

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