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InAs/GaSb Hot Electron Transistors Grown by Low-Pressure Metalorganic Chemical Vapor Deposition

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We have investigated an abrupt and a graded GaInSb collector and GaSb collector in LPMOCVD grown HETs and report the effect of the collector barrier on device performance. The device uses GaSb emitter barrier and 100Å-wide InAs base. Room temperature common-emitter current gain for GaSb barrier HET, the abrupt one,and the graded one are 0.5,1.2,and1.6,respectively. The collector barrier for the GaSb HET is the highest. The barrier for the other two cases are comparable. The grading reduces the quantum reflection to enhance collector current.

Introduction

Hot electron transistor concept[1] has been realized in the AlGaAs/GaAs system and investigated in a detail for decade. Recently, it has been realized that the AlGaAs system is not suitable for high performance HETs , due to the narrow Γ-L energy separation[2] Instead, InAs base was proposed. In 1987, room temperature operation of AlGaInAsSb HETs grown by MBE was demonstrated[3], but thereafter, little has been reported.

An InAs/GaSb heterostructure is unique since the conduction band in InAs lies 0.15 eV below the GaSb valence band[4] Nevertheless, the system has been little grown by MOCVD, so far[5]. We have recently observed a clear negative differential resistance in a structure of 300Å GaSb sandwitched between two InAs electrodes grown by MOCVD[6].

In this paper, we investigate an abrupt and a graded GaInSb collector and GaSb collector in LPMOCVD-grown HETs and report the effect of the collector barrier on device performance.

Experimental

Low pressure MOCVD was used. The pressure was 100 Torr. The reactants were TMGa, TMIn, TMSb, and 10% arsine. (100) Te-doped GaSb substrates were used. A schematic diagram for GaSb substrates were used. A schematic diagram for GaSb barrier HET is shown in fig.1. No buffer layer was grown. After undoped GaSb was grown directly on the GaSb substrate at 570℃, TMGa and TMSb were turned off and the substrate temperature was lowered. InAs was then grown at 470℃. TMIn was turned off and the substrate temperature was raised to 570℃ under an arsine atmosphere. Next, undoped GaSb was grown. The structure was completed by an n-GaSb. H_2Se was used for doping. As seen in fig.1, HET is a mesa structure. The emitter is 114 μm in diameter. The mesa was defined using RIE down to InAs base. Etching rate for GaSb and InAs is shown in Fig.2. Selectivity close to 100 enables one to etch down to, but not through, the base. A schematic energy band diagram is shown in fig.3. Electrons, which are injected from the emitter traverse the base ballistically and can be collected as long as no scattering occurs. Since the structure is symmetric, a high current gain can not be expected. $Ga_{0.9}In_{0.1}Sb$ of 200Å was inserted between the InAs and GaSb collector barrier to reduce the collector barrier for the abrupt one. To reduce the quantum reflection at the collector barrier, the collector was graded over 200 Å from GaSb to $Ga_{0.9}In_{0.1}Sb$ for the graded one.

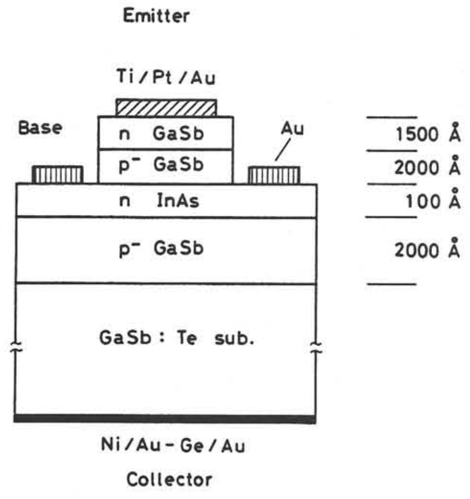

Fig.1 Schematic diagram of GaSb barrier HET.

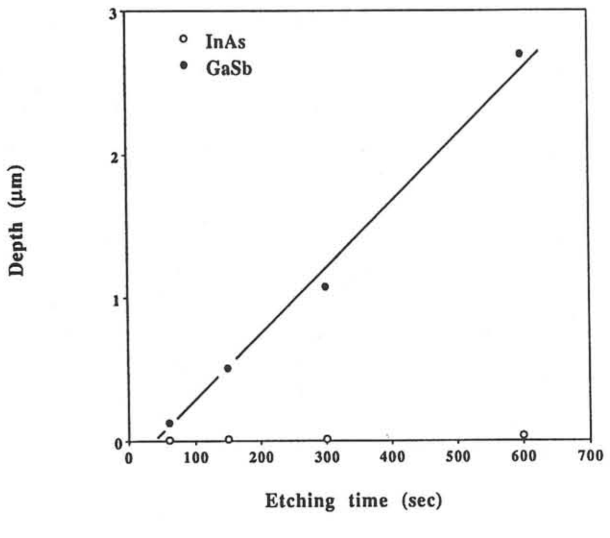

Fig.2 Etching rate for GaSb and InAs

Results and discussion

Room temperature common-emitter characteristics for the HETs are shown in Fig.4. The transistors show good electrical characteristics. Current gain for the GaSb HET, the abrupt one, and the graded one are 0.5, 1.2, and 1.6, respectively. The offset voltage is due to the difference in area of emitter/base and the base/collector junctions.

To gain deeper insight into the physics determining performance of the HETs, figure 5 shows I-V characteristics for the emitter/base and the base/collector heterojunctions. At high biases there is a departure in the emitter/base curves from ideality due to the voltage drop across the emitter contact resistance. Values of ideality factor are summarized in Table 1. Such values indicate that current is not only due to an emission of electrons over the barrier, which varies as exp qV/kT. Other mechanism, which varies as exp qV/nkT ($n \geq 1$) is required. By analogy with Schottky barrier, tunneling through the barrier and/or recombination in the barrier are the candidate. Such current cannot contribute the transistor operation and should be reduced. Current for the GaSb emitter/ InAs base junctions are comparable. For the base/collector junction, current for the GaSb HET is the least. The collector barrier for the GaSb HET is the highest. The barrier for the other two cases are comparable. For the GaSb barrier HET, current for the base/collector junction is 4 times as large as that for the emitter/base junction at V=0.3V, where n=1 current is dominant. Since the base area is 4 times as large as the emitter area, forward current density for the emitter/base and base/collector heterojunctions are comparable, indicating that the structure is symmetric as designed. Variation of I_c and I_b with V_{be} is shown in Fig.6. I_c varies as exp qV/kT. It has been confirmed that I_c is well described by thermionic emission. As seen in fig. 6, I_c is enhanced by grading. Since the barriers for the graded one are comparable with that for the abrupt one , this suggests that the grading reduces the quantum reflection to enhance I_c.

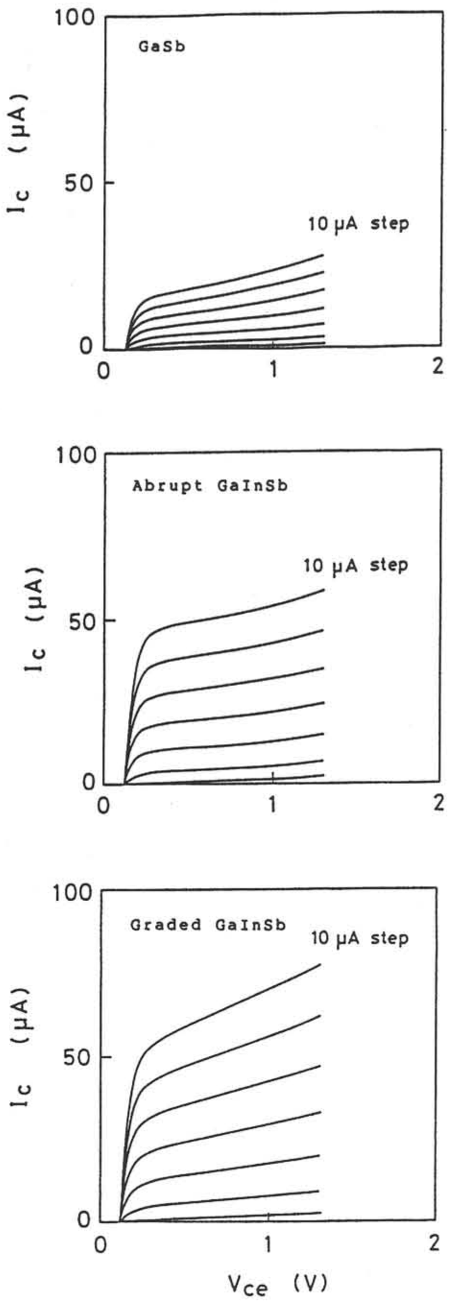

Fig.4 Room temperature common-emitter characteristics of (a)GaSb barrier,(b)abrupt GaInSb, and (c)graded GaInSb HETs.

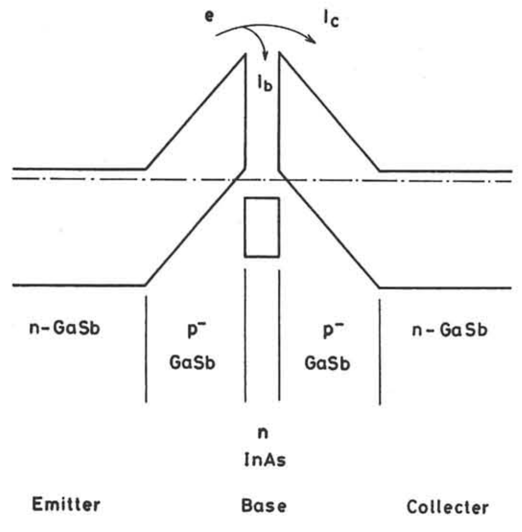

Fig.3 Schematic energy-band diagram of GaSb barrier HET.

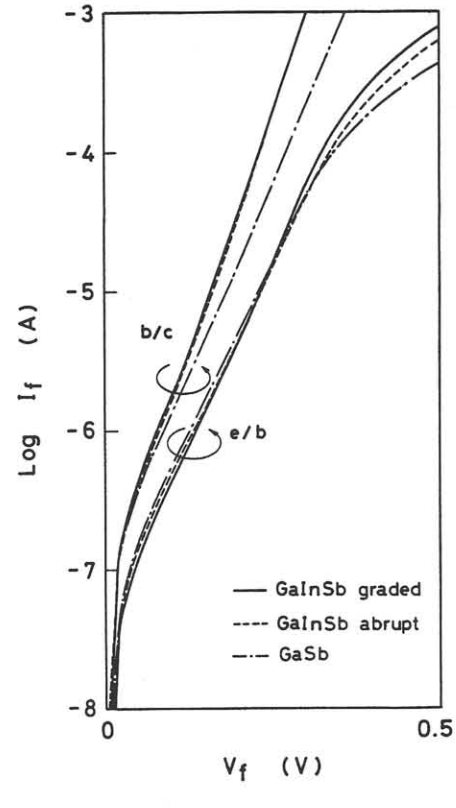

Fig.5 Forward I-V characteristics of the emitter/base and the base/collector heterojunctions.

Table 1 Ideality factor

	GaSb	Abrupt GaInSb	Graded GaInSb
e/b	1.8	1.7	1.5
b/c	1.5	1.2	1.2

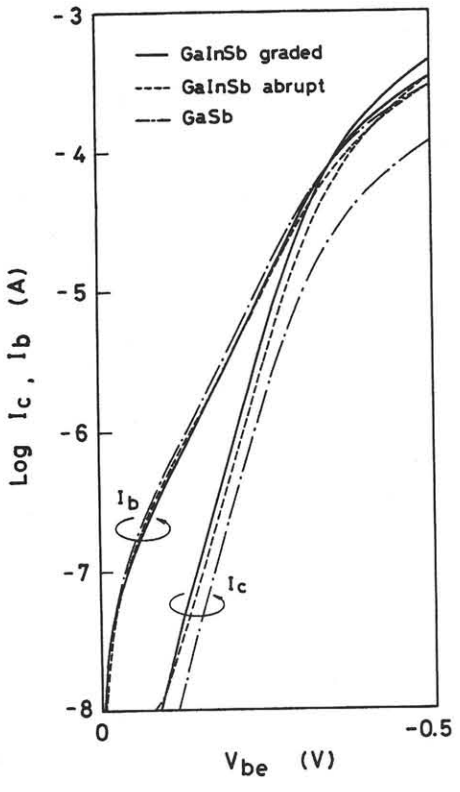

Fig.6 Variation of I_c and I_b against V_{be}.

Summary

Room temperature operation of LPMOCVD-grown HETs has been demonstrated. Common-emitter current gain is enhanced above 1. The preliminary data are promising.

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