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Fabrication and Characterization of InAs Channel Heterojunction Field-Effect Transistors

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We report on the fabrication and characterization of (AlGa)Sb/InAs quantum well heterojunction field-effect transistors based on molecular beam epitaxy (MBE). The MBE growth scheme dependence on the electrical characteristics of the InAs quantum well were investigated. A 1.7 μm gate length InAs channel FET with optimized heterostructure showed decent pinch-off characteristics and transconductance of more than 460 mS/mm (V_{ds}=0.5v) at room temperature. In higher lateral electric field region (V_{ds}>0.8v), much higher transconductance and drain current were observed with high output conductance. This phenomenon corresponds to the increased sheet carrier concentration under high lateral field observed in a separate set of experiments of pulsed high-field Hall-effect measurement.

I. INTRODUCTION

InAs channel field-effect transistors are potentially superior to (InGa)As channel MODFET's or GaAs channel MODFET's for their higher low-field mobility[1], higher-lying satellite valleys, deeper quantum well depth with suitable barrier materials, such as AlSb, or (AlGa)Sb. However, there has only been non-ideal results reported so far[2][3]. We have examined MBE growth schemes dependence on electrical characteristics of the as-grown samples and field-effect transistors. In an optimized heterostructure based on the MBE study, decent pinch-off characteristics were observed in an InAs channel heterojunction FET. Sudden drain-current increase at high drain voltage region (V_{ds}>0.8v) have been investigated by (i) pulsed high-field Hall-effect measurements and (ii) substrate current measurements in a different heterostructure where 1μm of conductive GaSb layer is inserted in the buffer layer.

II. MBE GROWTH

Main focus of this section is the aluminium compositional dependence of the barrier layer on the electrical characteristics of the InAs channel. The heterostructure under investigation has a sequence of layers as GaSb[100Åcap], (AlGa)Sb [150Å top barrier], InAs [150Å channel], (Al_XGa_{1-X})Sb [2000Å lower barrier], AlSb [2.8μm buffer], from top to bottom. The layers have been grown by molecular beam epitaxy on semi-insulating GaAs substrate which is lattice mismatched to InAs/(AlGa)Sb system by more than 7%. The thick AlSb buffer layer helps to improve crystal quality of the InAs channel layer which otherwise gets worse. The aluminium composition of the upper barrier had little effect on the electrical characteristics of the channel. Thus, we have kept 50% of aluminium in the upper barrier for our entire experiment so that unwanted reaction with the atmosphere can be reduced while maintaining high barrier height for electrons. When the aluminium composition of the lower barrier of the InAs channel is unity, i.e., x=1, both mobility and sheet carrier concentration become highest. A typical Hall-effect measurement results are shown in Fig.1. Upon light illumination, the mobility and the sheet carrier concentration at 77°K have been slightly reduced. Much more enhanced negative photoconductivity has been observed in InAs/AlSb[1] heterostructures. This negative photoconductivity[1] is presumably due to the trapped electrons in the barrier layer or at the InAs/AlSb interface[4] and the subsequent reconstruction of the band bending after the light illumination. As the aluminium composition were decreased, monotonic decrease of both mobility and sheet carrier concentration were observed. At x=0.5, sheet carrier concentration were 70% and 50% of that of x=1 case at 300°K and 77°K, respectively. The electron mobility were 80% and 35% of that of x=1 case at 300°K and 77°K, respectively. This result suggests higher deep donor concentration in (Al_XGa_{1-X})Sb with higher x.

The mobility reduction at lower x samples may be caused by the reduction of the screening effect because of the lowered carrier concentrations, but it is not entirely clear at present. These results suggest to use higher aluminium composition, x, in the lower barrier of the InAs channel. On the other hand, lower x is preferable for the simpler device fabrication process and for the increased device reliability. In order to meet both requirements, a compromised structure is proposed and fabricated as explained in the next section.

III. FABRICATION OF THE OPTIMIZED FET STRUCTURE

As shown in Fig.2, the optimized heterostructure layers consist of 2.8μm AlSb buffer layer, 2000Å of $(Al_{.5}Ga_{.5})Sb$ buffer layer, 60Å of AlSb layer, 150 Å of InAs channel, 150 Å of $(Al_{.5}Ga_{.5})Sb$, and 100 Å of GaSb cap layer. The inserted 60Å of AlSb was intended to provide increased carriers to the channel from the not-intentionally doped donors in the AlSb[1] or at the InAs/AlSb interface[4]. The Hall-Effect measurements by van der Pauw method showed room temperature mobility ranging from 14500 cm^2/Vs to 16200 cm^2/Vs and low temperature mobility ranging from 32700cm^2/Vs to 38200cm^2/Vs at 77°K . The corresponding sheet carrier densities ranged from 1.48 $x10^{12}$ cm^{-2} to 2.04 $x10^{12}$ cm^{-2} at room temperature. At 77°K, the corresponding sheet carrier concentration ranged from 1.22 $x10^{12}$ cm^{-2} to 1.38 $x10^{12}$ cm^{-2}. The average sheet resistances were 223Ω/□ and 139Ω/□ measured at 300°K and 77°K, respectively. The present structure with thin AlSb layer inserted under the InAs channel showed suppressed negative photoconductivity effect as was the case for AlGaSb/InAs/AlGaSb structures without AlSb thin layer. The mechanism is not clear at present, but it seems to be suggesting that the InAs/AlSb interface[4] is unrelated to the negative photoconductivity effect as long as the thick AlSb buffer (no GaSb buffer) is used. The standard fabrication procedure was employed: device isolation done by phosphoric-acid-based etchant, AuGe/Au as ohmic metal, and 1500Å of Au as a Schottky gate metal without gate recess etching. All metals have been deposited by thermal evaporation.

IV. OPTIMIZED FET RESULTS

As shown in Fig.3, 1.7 μm gate length InAs channel FET showed good pinch-off characteristics with threshold voltages of -0.15 v(V_{ds}=0.5v) to -0.3 v(V_{ds}=1v). These results show better pinch-off characteristics than those reported before[2][3]. The thin AlSb layer together with 2000Å of $(Al_{.5}Ga_{.5})Sb$ buffer layer which presumably contains much less deep donors as suggested by the MBE study (section II.) are probably contributing to obtain the decent pinch-off characteristics. One also notices a kink effect similar to what is commonly observed in short channel MODFET's[5] or SOI devices[6]. The measured ohmic contact resistance by Transmission Line Model (TLM) was about 0.2Ωmm. The drain current and the transconductance versus gate voltage of a 1.7μm device is shown in Fig.4. The maximum (extrinsic) transconductance was 509mS/mm (1.7μm FET) at room temperature measured at V_{ds}=1 volt. The output conductances, g_d, at the high V_{ds} region (V_{ds} > 0.8v) become as high as 200mS/mm. Our results may suggest that in the InAs channel FET, the impact ionization occurs in relatively long gate length (1.7μm) devices, reflecting the narrow bandgap energy of InAs. The measured maximum transconductance at much lower output conductance region (V_{ds}=0.5 v) was 460 mS/mm which is still high for 1.7μm gate length device. The drain current capability was 300mA/mm with this 1.7μm device. The field-effect mobility of 5000 cm^2/Vs and the K-factor (= $\partial g_m/2\partial V_g$) of 1450mS/Vmm have been obtained at room temperature. The transconductance dependence on gate lengths in various MODFET's are shown in Fig.5. The comparison indicates that the present device is a candidate of high performance MODFET beyond InGaAs channel MODFET's. The high transconductance probably comes from the high electron velocity and the increased carrier concentration. The mobility modulation[7] effect by vertical electric field application could be of some assistance to obtain high transconductance. In order to investigate the mechanism causing the high transconductance at modest drain voltage region and enhanced drain current in high drain voltage region, substrate current and high field pulsed Hall-effect measurement experiments have been performed as described below.

V. NEW STRUCTURE AND SUBSTRATE CURRENTS

In order to examine the possibility of impact ionization, substrate currents were measured in a new structure explained below. This was achieved by inserting 1μm of conductive GaSb buffer layer(p-type) under the 0.7μm of AlSb buffer layer. Layers above AlSb buffer is identical to the structure explained in sectionsIII and IV. For the fabrication of FET's, almost identical process procesure described above was taken except ohmic contact

process. Top capping GaSb layer and the (AlGa)Sb upper barrier layer were chemically etched and a metal layer (gold) was deposited directly on the InAs channel layer by thermal evaporation to make a non-alloyed ohmic contact. The selective etching was done by using the ammonium hidroxide based etchant. The new structure with an alternative buffer scheme showed improved surface morphology and higher low-field mobility probably because of the high surface migration of Ga atoms during the growth. Low-field electron mobility of 17000 cm^2/Vs and 80300cm^2/Vs were obtained at 300°K and 77°K, respectively. In Fig.6, substrate currents flowing into the GaSb buffer layer are shown together with the drain currents. This figure shows that there are some amount of holes flowing into the substrate but the amount of the current is more than three orders of magnitude smaller than that of the drain current. Thus, it is unlikely that the increase of the drain current at high lateral field is caused by the impact ionization. Another possibility of parasitic bipolar action might be denied due to the fact that there is no negative resistance observed in the I-V characteristics which is commonly seen in n-MOS under parasitic bipolar action.

VI. PULSED HALL-EFFECT MEASUREMENTS

A Hall-bar sample of the same heterostructure as was explained in the previous section has been studied. The structure is the same as in the previous section except that no gate metal was deposited to avoide the possible gate leakage problem. The drain to souce distance of the high-field Hall bar sample was 50μm. Measured electron velocity and carrier concentration as a function of the lateral electric field are plotted in Fig.7(a) and (b), respectively. One notices that the carrier concentration increases at high electric field region and that the velocity saturates quickly to around $1.5x10^7$cm/s. These results indicate some mechanism of carrier multiplication at high vertical field and velocity suppression, but the physics behind is not clear at present. The high low-field mobility and high sheet carrier concentration are the two factors that are contributing to the high transconductance of our device.

VII. CONCLUSIONS

InAs channel heterostructure has been optimized by MBE study and high performance InAs channel FET's have been successfully fabricated and characterized by dc FET characteristics and pulsed Hall-effect measurements. Both high low-field mobility and high sheet carrier concentration are found to be contributing to the high transconductance of the present device.

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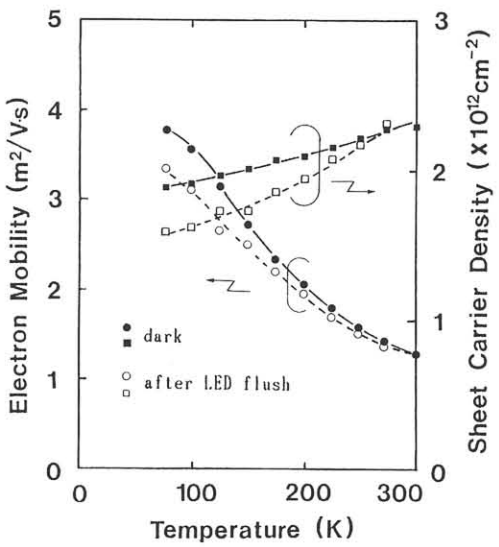


Fig.1 Electron mobility and sheet carrier concentration in a (AlGa)Sb/InAs quantum well.

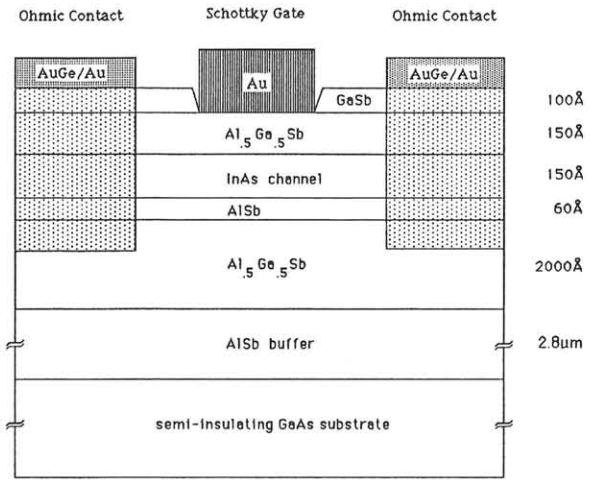


Fig.2 Schematic diagram of an InAs channel heterojunction transistor.

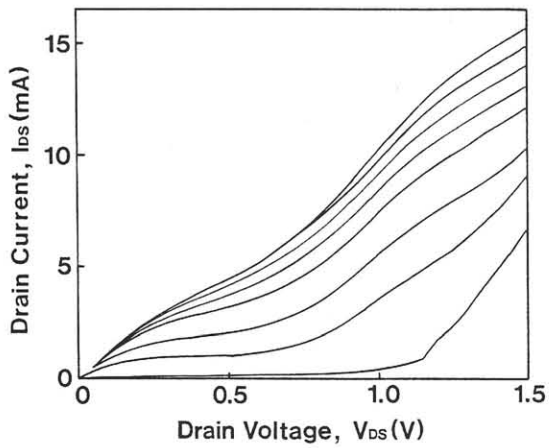


Fig.3 Measured drain current characteristics of the 1.7μm (gate length) InAs FET at 300K. The gate voltages are taken from -0.1 volt to 0.25 volt by 50mV step.

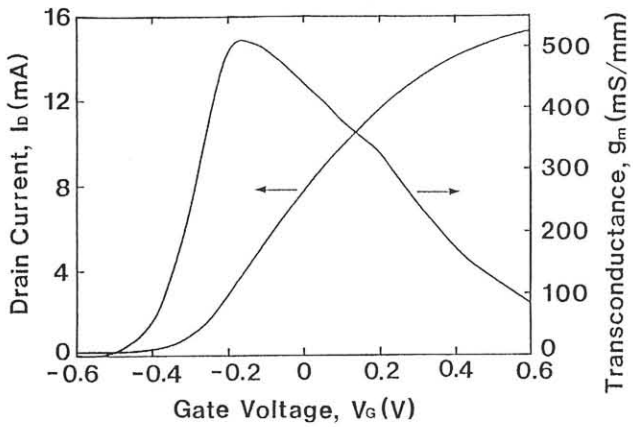


Fig.4 Measured drain current and transconductance dependence on gate voltage at 300K. The drain to source voltage was taken to be 1 volt. The channel length and channel width are 1.7μm and 50μm, respectively.

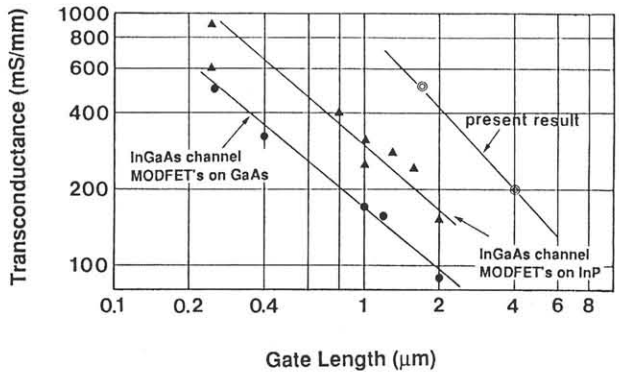


Fig.5 Comparison of transconductance versus channel length in various heterostructures. Solid circles denote InGaAs channel MODFET's lattice-mismatched to the GaAs substrate. Solid triangles denote InGaAs channel MODFET's lattice-matched to the InP substrate.

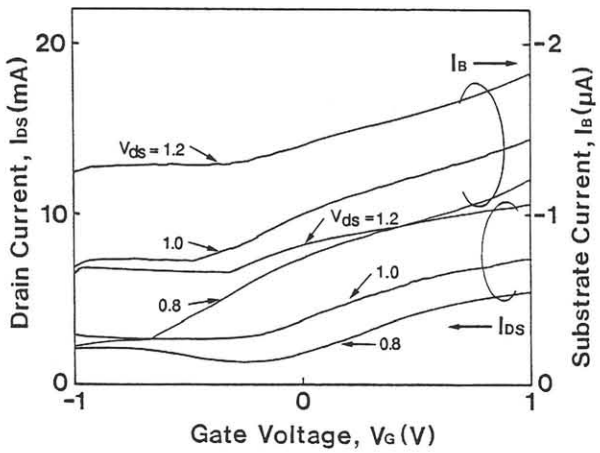
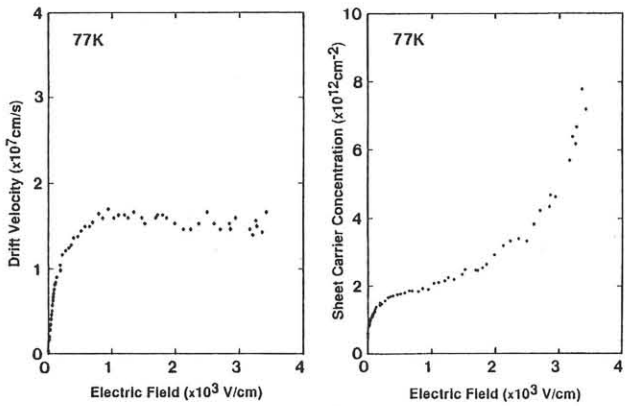


Fig.6 Substrate current and drain current characteristics of an InAs channel FET(L_g=1.0μm). Drain voltage is taken as a parameter.



(a) (b)

Fig.7 Drift velocity(a) and sheet carrier concentration (b) of an(AlGa)Sb/InAs quantum well measured by pulsed high-field Hall-effect measurements.