Extended Abstracts of the 22nd (1990 International) Conference on Solid State Devices and Materials, Sendai, 1990, pp. 71-74



# A Triple-Level Interconnection Technology for High Speed 16 Kb GaAs SRAM

M.Noda, S.Matsue*, M.Sakai, K.Sumitani, H.Nakano, T.Oku, H.Makino*, K.Nishitani and M.Otsubo

Optoelectronic and Microwave Devices R & D Lab., LSI R & D Lab*. Mitsubishi Electric Corporation

4-1, Mizuhara, Itami, Hyogo 664, JAPAN

A triple-level Au-based interconnection technology was developed in order to reduce the wiring length and chip size for realizing high speed 16Kb GaAs SRAM with high yield. Two of its major features are 1)A wafer rotating ion-milling with inclined ion-beam for fine pattern delineation and 2)Low temperature P-CVD for suppression of hillocks at the edges of the interconnection metal. Using this technology, the wiring length and chip size were reduced to 69% and 58%, respectively, of those we previously reported. As a result, 16Kb SRAMs with maximum address access time of less than 5ns and typical power dissipation of 2W were realized at the temperatures ranging from 25°C to 100°C. Wafer yield as high as 10% was also obtained.

## 1. Introduction

Up to now, 16Kb GaAs SRAM having a maximum address access time of 7ns with an excellent soft error immunity has successfully been developed[1]. However, the operating speed doesn't compete with that of Si ECL RAMs and the chip yield is poor. To improve the speed and yield, it is necessary to reduce the wiring length and chip size. For this purpose, multi-level interconnection such as triple-level interconnection is quite effective, especially when the third level metal is used for power bussing. Further, the pattern layout of signal lines at lower levels becomes easier and integration feasibility can be increased.

In spite of the above merits, the triple-level interconnection gives rise to a demerit, which is additional capacitance due to the cross-over between the third level metal and lower level metals. Therefore, to achieve high speed operation, the wiring length must be shortened so as to keep the shortening effect larger than that of the additional cross-over capacitance. Since access time(tacc) for SRAMs depends on the interconnect capacitance, it is important to examine a relationship between the wiring length and the additional capacitance.

In this paper, using a simple model of interconnection, we first calculate the reduction ratio of the length of signal lines for the triple-level interconnection vs. that for the double-level one. We show that the calculated values are comparable to those obtained by SPICE2 simulation. We then describe in details our triple-level interconnection technology. Finally, we present the performances of 16Kb GaAs SRAM fabricated with this technology.

## 2. Access Time Consideration

Trade-off between reduced interconnect capacitance and additional one due to the third level metal is examined . Figure 1 shows simplified models of both double and triple level interconnections. We assume that interconnect capacitance per unit length is the same for all the cases of (1)between the 1st and 2nd-level interconnections, (2)the 2nd and 3rd, and (3)the 1st one and substrate, and it is denoted by C. We also assume the same resistance per unit length for each level metal, which is denoted by R. The wiring lengths for the 1st and 2nd level are denoted by $l_1$ and $l_2$, respectively. The delay time, $t_1$, through signal line $l_1+l_2$ for double-level interconnection is written approximately as

$$t_1 \sim (Rl_1+Rl_2)(2Cl_1+Cl_2) = RC(l_1+l_2)(2l_1+l_2) \quad (1)$$

The delay time, $t_2$, for triple-level interconnection is given by

$$t_2 \sim (R\alpha l_1 + R\alpha l_2)(2C\alpha l_1 + 2C\alpha l_2) = 2\alpha^2 RC(l_1+l_2)^2 \quad (2)$$

where $\alpha$ is a given reduction ratio.
From the above equations and $l_1 \sim l_2$ in our design,

$$t_2/t_1 \sim 4\alpha^2/3 \quad (3)$$

In order to achieve a smaller delay time for triple-level interconnection than for double-level interconnection, this equation implies that the reduction ratio must be smaller than $\sqrt{3/4}$, which is approximately 87%.

Note that using the same design rule, the total wiring length $l_1+l_2$ can be reduced at the design level from 28.6mm to 19.8mm by applying the triple-level interconnection. The reduction ratio is 69%, leading to a smaller access time expected. In this case, we have $t_2/t_1 = 64\%$ from eq.(3). On the other hand, we performed a circuit simulation with SPICE2 for the RAMs with triple-level and double-level interconnection. As shown in Fig.2, the value of $t_2/t_1$ is 57%, which is derived from the ratio (4.0ns-2.4ns)/(5.2ns-2.4ns). Since this value is close to the calculated one, our simple model is useful to obtain relative delay time ratios.

## 3. Triple-level Au-based Interconnection Technology

A technology for triple-level interconnection using lift-off process has been reported[2]. However, the lift-off technique is not adequate for LSI interconnection because 'naps' often appear at the edge of interconnection metal, which causes leakage between the interconnections. Our proprietary triple-level interconnection technology is based on the sputter and etching(ion milling) and consists of 3-steps. 1)A Au/Ti double metal layer is sputter-deposited, followed by ion milling delineation, 2)planarization of the insulator(SiON) between interconnections is performed by Spin On Glass(SOG) and etch-back techniques, and 3)through-holes are formed by RIE.

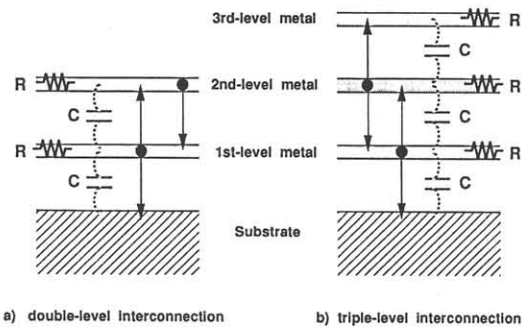


Fig.1 Assumption for interconnect capacitance

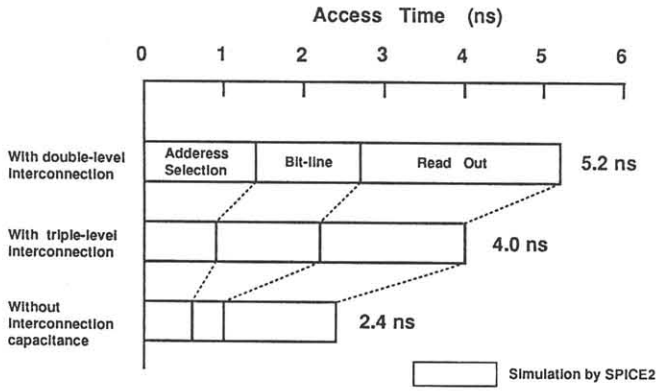


Fig.2 Contents of access time calculated by SPICE2

### 3-1 Ion milling technique

The ion milling has been used to delineate Au-based interconnection metals[3]. Its major features are that 1)etching rate depends on the incident angle of ion beam and 2)selectivity is relatively small. In general, the etching rate is highest at ion beam angle($\theta$) of ~60° measured from the normal direction. 'Facets' appear at this ion beam angle when the incident angle is 0°. This results in a triangle shape and causes higher interconnection resistance.

Therefore, the angle is required to be optimized from the viewpoint of getting rectangular shape. An optimum incident angle of ion beam exists, which depends on the initial cross-sectional shape of resist. The angle dependence of etched shape is examined in detail and 30° is found to be optimum. SEM photographs of the ion milled patterns are shown in Fig.3. It is found that at incident angle of 0°, a 'facet' plane of triangular shape is clearly seen. At 30° angle, the side of resist pattern is kept steep and the shape is closer to rectangular.

A cross-sectional view of the newly developed triple-level metal interconnection is shown in Fig.4. Minimum line and space, and minimum hole size are 1.5$\mu$m and 1.5$\mu$m, and 1.6$\mu$m x 1.6$\mu$m, respectively. In the design, the second level metal can contact directly with both gate and ohmic metal, which is very effective to reduce memory cell size and chip size. The third-level metal is well planarized.

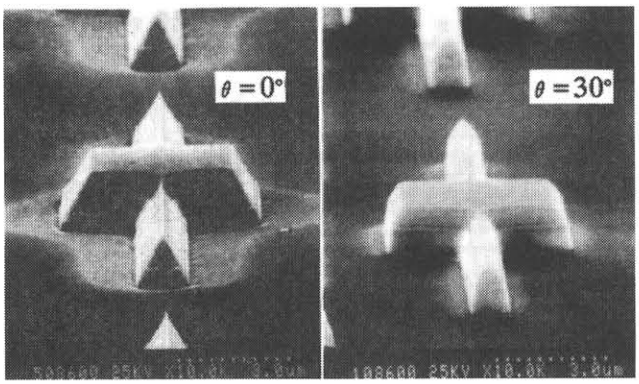


Fig.3 SEM photos of ion milled patterns

3-2 Suppression of hillock generation

Leakage between the upper and lower interconnections has often been observed. It is also found that defects exist on the surface of lower interconnection metal, especially at its edges. The defects were analyzed with SEM and micro-Auger spectroscopy. Figure 5 shows an SEM photograph of the defect found at the edge. As seen from the figure, grain boundaries appear in and around the defect. Micro-Auger spectra in and around the defect showed no significant difference. These results lead us to conclude that the defect is generated from the Au interconnection itself. To investigate a mechanism of the hillock generation, the dependence of hillock density on process temperature was examined. Figure 6 shows hillock density versus deposition temperature of upper insulator. As the temperature decreases, the density decreases remarkably. The hillock density at 250°C decreases down to less than 6% of that at 300°C. As in the case of Al, the hillock seems to occur so as to release the stress at metal edges. As expected, it was confirmed that the stress increases as the anneal temperature increases. Therefore, the stress enhancement is the origin of the hillock generation. The activation energy($E_a$) of generating hillock is 1.50eV. This value is lower than the $E_a$ of atomic diffusion of Au in bulk(1.81eV). It is likely that the diffusion occurs through grain boundary of sputtered film. From these results, the deposition temperature was lowered to 250°C. Distributions of failed 16Kb SRAM chips caused by the leakage are shown in Figs.7(a) and (b) for the temperatures of 300°C and 250°C, respectively. It is apparent that the failure decreases remarkably by lowering the temperature.

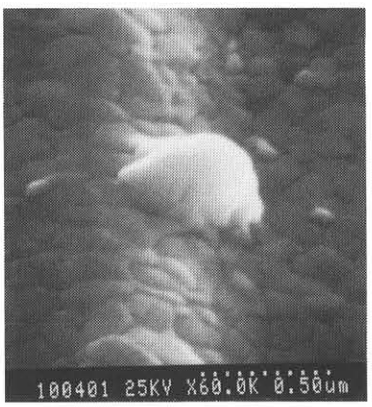


Fig.5 SEM photo of hillock on Au-based metal

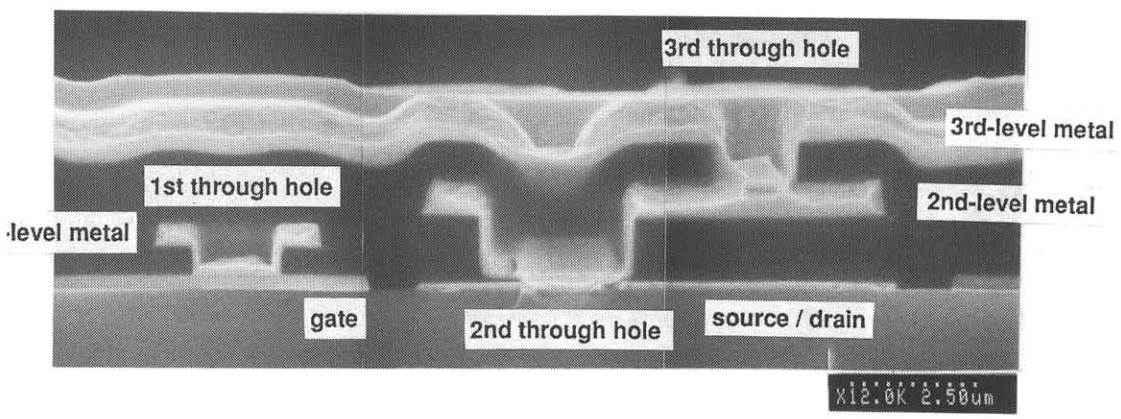


Fig.4 SEM photo of cross-sectional view of triple-level metal interconnection

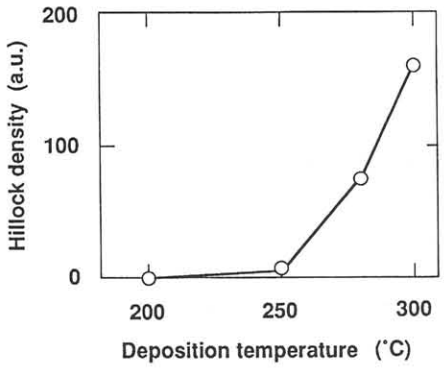


Fig.6 Hillock density vs. deposition temperature

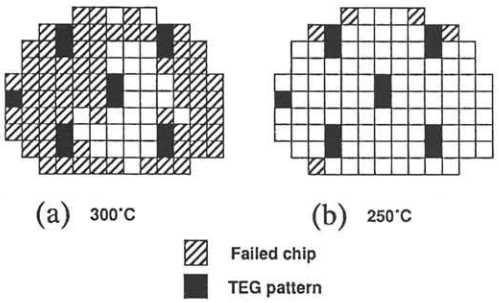


Fig.7 Failed 16Kb SRAM chip distribution by leakage between interconnections over 3-inch wafer

## 4. Performance of 16Kb GaAs SRAM with Triple-level Interconnection

By using the interconnection technology described above and 0.7$\mu$m gate BPLDD-FETs[4], high-speed and high-yield 16Kb SRAMs have successfully been realized. Figure 8 shows a microphotograph of the 16Kb SRAM. A typical distribution of address access time(tacc) measured by the galloping test pattern is shown in Fig.9. Maximum tacc is less than 5ns and typical power dissipation is 2W. In practical use, the RAM is required to operate in a wider temperature range. In the range from 25°C to 100°C, the RAMs operated stably and the access time was kept less than 5ns. At 100°C, maximum tacc is as small as 4.4ns with the power dissipation of 2W. High speed and stable operation are achieved even in the harsh environment of temperature as high as 100°C. Wafer yield as high as 10% is also attained.

## 5. Conclusion

We have introduced new triple-level metal interconnection technology in order to reduce the interconnect capacitance of 16Kb GaAs SRAMs. The chip size is shrunk down to 58% of that for the RAM with double-level interconnection[1]. The RAMs with maximum address access time of less than 5ns and typical power dissipation of 2W were realized with a wafer yield as high as 10%. They are also confirmed to operate with a wide temperature range between 25°C and 100°C.

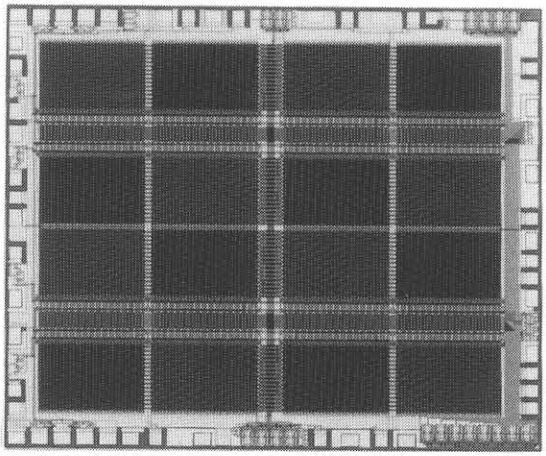

Fig.8 Photo of 16Kb SRAM with triple-level interconnection

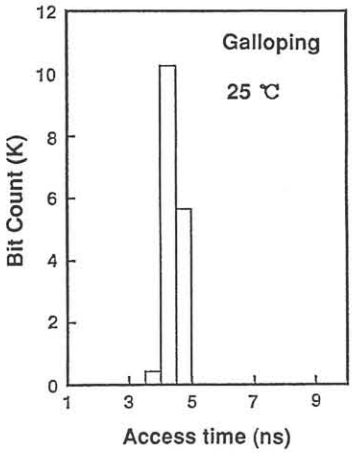


Fig.9 tacc distribution of 16Kb SRAM

## Acknowledgement

The authors wish to thank Drs.K.Fujikawa and S.Kayano for their continuous encouragements and useful advice.

## References

1)S.Matsue,H.Makino,M.Noda,N.Tanino,S.Takano, K.Nishitani and S.Kayano; IEEE GaAs IC Symp.Tech.Dig., 1989, p41
2)N.Kato,M.Hirayama,K.Asai,Y.Matsuoka,K. Yamasaki and T.Ogino;IEDM Tech.Dig.1985,p90
3)N.Tanino,S.Takano,M.Noda,H.Makino,K.Sumitani, H.Nakano K.Nishitani and S.Kayano; IEEE GaAs IC Symp.Tech.Dig., 1986, p101
4)M.Noda,K.Hosogi,K.Maemura,T.Kato,Y.Nakajima, K.Nishitani and M.Otsubo; Proc.Int.Symp.GaAs and Related Compounds,Japan, 1989, p653