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Extreme Low Power 1:4 Demultiplexer Using Double Delta Doped Quantum Well GaAs/AlGaAs Transistors

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A 1:4 demultiplexer circuit has been developed and fabricated using a recessed gate process for enhancement and depletion transistors with 0.5µm gate length based on a double-delta-doped- quantum well GaAs/AlGaAs structure. The process shows a gate delay of 25 ps at 0.5 µm gate length and 16 ps at 0.3 µm gate length. The demultiplexer was designed in Direct Coupled FET Logic (DCFL). First measurements show a data rate of 4 Gbit/s and a power consumtion of 165 mW at 1.5V supply voltage, which is the lowest value published for comparable data rates. This includes five 50 Ohm buffers with 0.8V output voltage swing. A design using 0.3 µm gate length is in process.

1. INTRODUCTION

There are increasing demands for high speed or low power consumption characteristics for LSI's. Gigabit-per-second optical fibre communication systems, high speed instrument systems and portable telecommunications systems are some of the most interesting applications.

GaAs is considered to be the most realizable solution for these integrated circuits. And DCFL is the most promising candidate for both, large scale integration as well as low power consumption. For this purpose several multiplexers and demultiplexers have been developed in recent years (see ref. [1] to [4]).

This paper describes circuit design, fabrication and measurements of an 1:4 demultiplexer, which is a key element for high speed communication systems.

2. TECHNOLOGY

The demultiplexer was fabricated by using a recessed gate process for enhancement and depletion heterostructure transistors. The vertical structure, shown in fig. 1, was grown by molecular beam epitaxy. The double-delta-doped quantum well transistor exhibits charge carrier concentrations in the order of $1.8 \times 10^{12}/cm^2$ and electron mobilities of 6000 cm^2/Vs at room temperature. The 0.5 µm gates are patterend using electron beam lithography. The threshold voltages for enhancement and depletion transistors are controlled by the two etch stop layers. Using selective RIE for the gate recess, an excellent threshold uniformity is obtained with a standard deviation of 10 mV across a 2" wafer. The measured transistor characteristics are given in table I.

Table I

	EFET	DFET
V_{th}	0.1 V	-0.5 V
g_m	470 mS/mm	380 mS/mm
R_s	0.7 Ohm mm	0.7 Ohm mm
f_t	26 GHz	27 GHz

3. CIRCUIT DESIGN

A block diagram of the 1:4 demultipexer is shown in fig. 2, a chip photograph in fig. 3. It consists of a 1:2 frequency divider for timing purposes, three pre-registers and four output registers as well as five output drivers. From the 1:2 frequency divider, four sequential latch pul-ses are derived for data acquisition. Together with the fourth data bit, the three preregistered bits are transfered to the output registers.

The circuit was designed by using DCFL with a ratio of enhancement to depletion gate width of two. The output drivers are super-buffered inverters driving a 50 Ohm load with a voltage swing of 0.8 V. The circuit consists of more than 200 transistors and the chip size is 1.0mm x 1.0mm.

4. RESULTS

The typical DCFL power dissipation at V_{dd} = 1.5 V is about 1 mW/gate.

On-wafer full logic functional tests were performed at a data rate of 100 Mbit/s. Fig. 4 shows the timing diagram for an 100% test. The chip yield was between 60% and 80%. Most failures showed a single punctual failure mechanism.

First results on high speed on-wafer tests showed a maximum data rate of 4.0Gbit/s (see fig. 5). The circuits were fully functional at a supply voltage above 1.0 V. The maximal usable data rate was nearly independent on the applied supply voltage in the region between 1.5 V and 3.0 V (see fig. 6). At 1.5 V supply voltage the power consumption was 165 mW and was nearly independent on the applied data rate.

5. SUMMARY

A 1:4 demultiplexer was designed and successfully fabricated using recessed gate heterostructure technology with half micron gate length. The chip consists of more than 200 transistors. A high speed operation of 4 Gb/s at a extreme low power dissipation of 165 mW was attained.

6. REFERENCES

[1] M. Okhata et al., "11Gb/s multiplexer and demultiplexer using 0.15 µm GaAs MESFETs" Int. Symp. GaAs and Rel. Comp., Karizuwa, Japan, 1989.

[2] H. Nakamura et al., "2GHz Multiplexer and Demultiplexer Using DCFL/SBFL Circuit and the Precise Vth Control Process", GaAs IC Symp., 1986.

[3] Y. Hatta et al., "A GaAs IC Set for Full Integration of 2.4 Gb/s Optical Transmission Systems", GaAs IC Symp., 1988.

[4] K. Ishida et al.,"12 Gbps GaAs 2-bit Multiplexer/Demultiplexer Chip Set for the SONET STS-192 Systems", GaAs IC Symp., 1989.

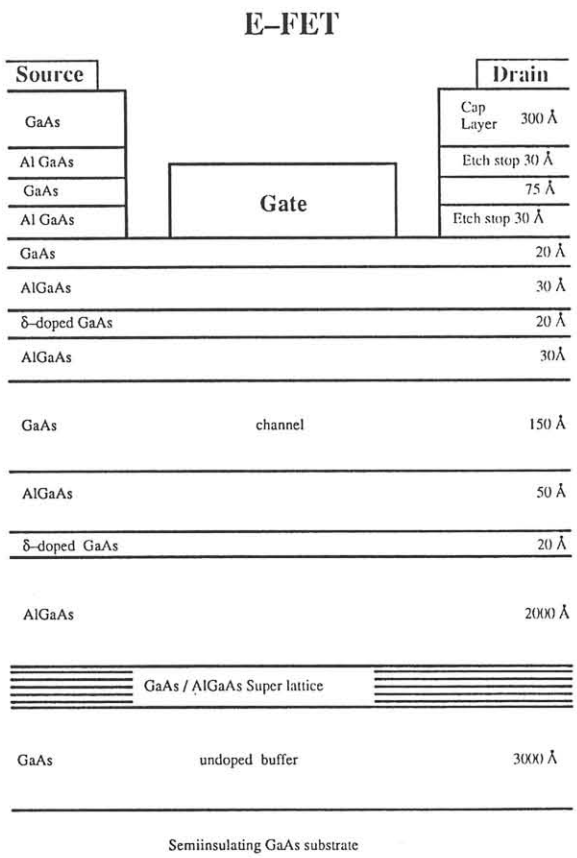

Fig. 1 Scematic cross section through an enhancement transistor.

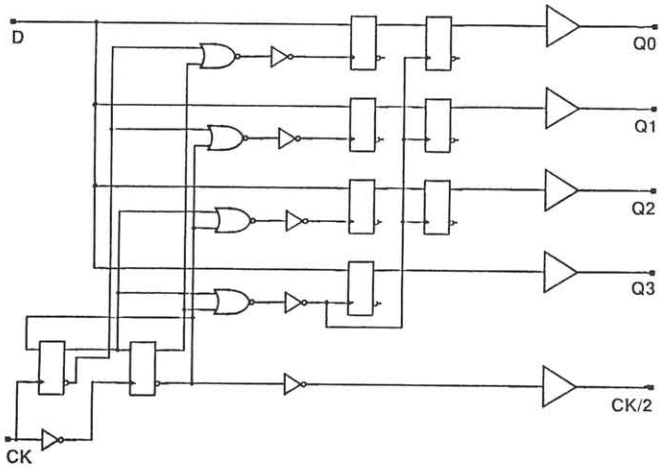

Fig. 2 Block diagram of the demultiplexer.

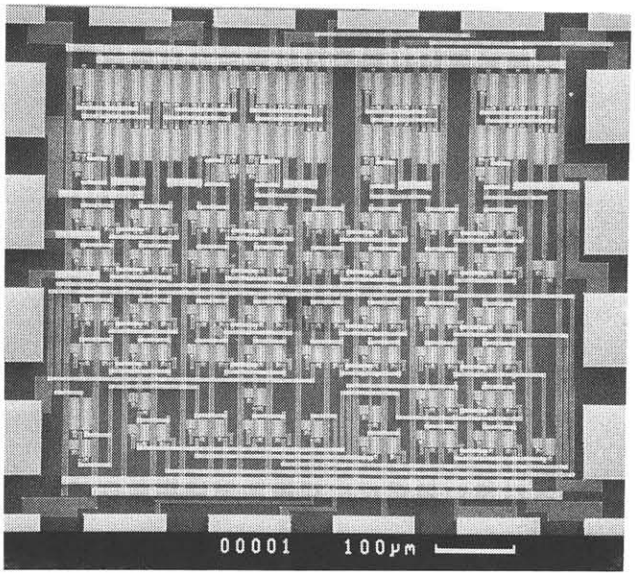

Fig. 3 1:4 demultiplexer die photograph.

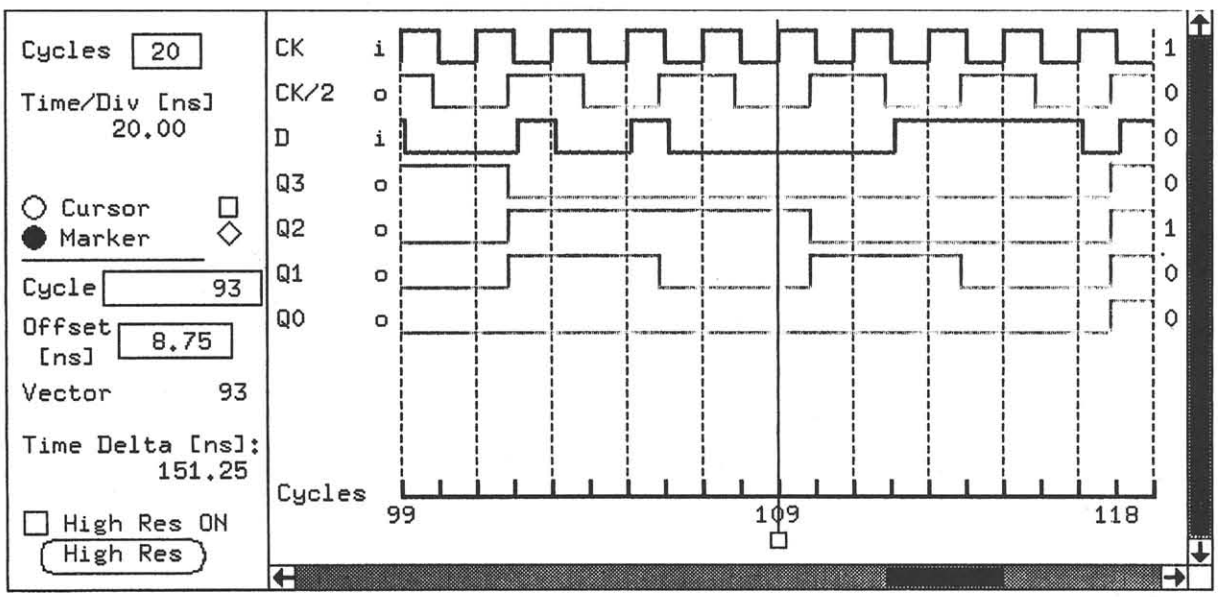

Fig. 4 Timing diagram of the 100 Mbit/s logic functional test

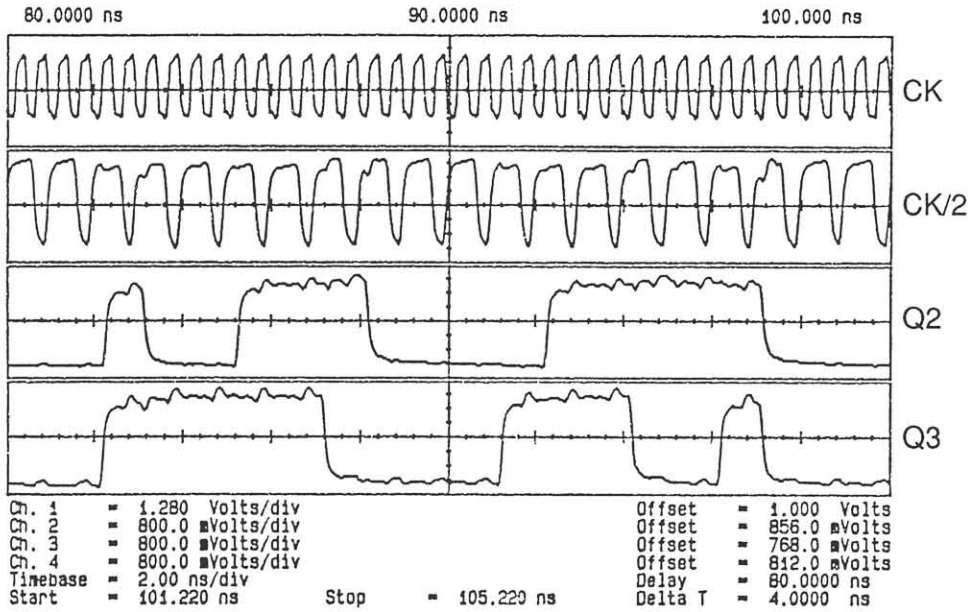

Fig. 5 Timing diagram of the high speed test. Only four signals are shown: clock input **CK**, clock output **CK/2** and the two paralell data output signals **Q2** and **Q3**.

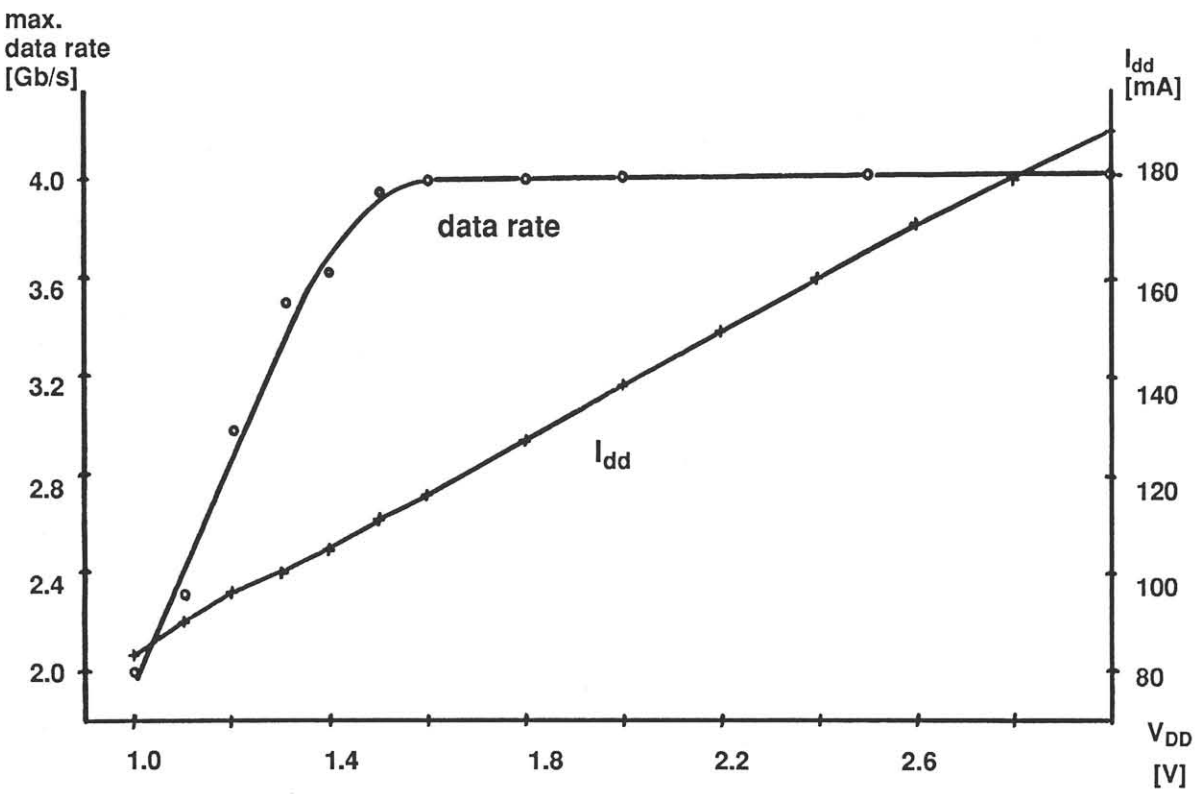

Fig. 6 Maximum processed data rate and supply current versus supply voltage