Extended Abstracts of the 22nd (1990 International) Conference on Solid State Devices and Materials, Sendai, 1990, pp. 83-86

A Sub-10 ps/Gate DCFL Circuit with 0.2 μm-Gate GaAs MESFET

Hiromi TSUJI, Hiroki I. FUJISHIRO, Hiroshi NAKAMURA, and Seiji NISHI
Research and Development Group, Oki Electric Industry Co., Ltd.
550-5 Higashiasakawa, Hachioji, Tokyo 193, Japan

A 0.2μm-gate buried p-layer MESFET using a new gate fabrication technique is reported. With this technique, the gate length can be easily reduced down to less than 0.2μm. The source resistance of enhancement mode FET can be also reduced resulting in excellent DC and RF performances. The maximum transconductance of 648mS/mm at a gate voltage of 0.6V and K-value of 506mS/Vmm were obtained. The maximum cut-off frequency was as high as 96.1GHz. The propagation delay time of 8.1ps/gate was observed with a power dissipation of 1.7mW/gate at a supply voltage of 1V.

1. Introduction

Recently, demands for high speed and low power consumption in digital ICs are increasing, and various kinds of devices have been proposed and demonstrated for these ends [1-5]. Among these devices, GaAs direct-coupled FET logic (DCFL) circuit is regarded as one of the most promising candidates because both the high speed and low power consumption can be realized at the same time. In DCFL circuits with GaAs MESFETs, reduction in the gate length is the most effective method to achieve excellent performances.

We have already reported a gate fabrication process to realize very short gate length and have applied it to AlGaAs/InGaAs pseudomorphic HEMTs in processing microwave devices [6].

In this paper, an improved fabrication technique is described. A 0.2μm-gate formation is demonstrated using a combination of bilayer-photoresists and an angle evaporation accompanied by stepped recess structure, which results in a low source resistance. Buried p-layer GaAs MESFETs are fabricated using this technique for the first time which show excellent DC and RF characteristics. The propagation delay time is also measured using a 19-stage DCFL ring oscillator.

2. Crystal Growth and Device Fabrication

The BP-MESFETs were fabricated on the wafers grown by molecular beam epitaxy on 2-inch HB semi-insulating GaAs substrates. A schematic cross section of the device structure is shown in Fig. 1. A thin p-layer was introduced under the channel layer to suppress the short channel effect.

Before the gate fabrication, each device was

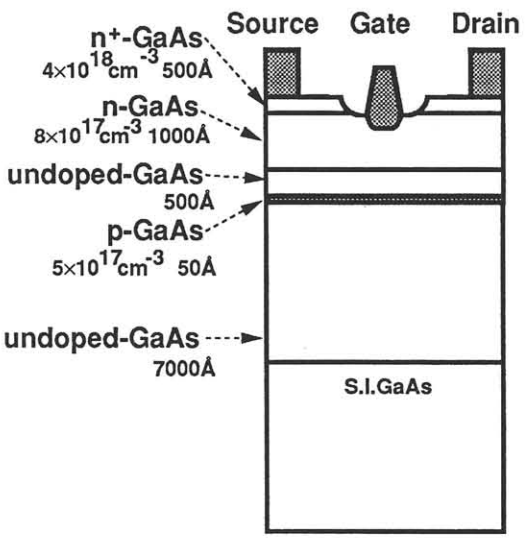

Fig.1 Schematic cross section of the buried p-layer MESFET.

isolated by oxygen ion implantation and source and drain ohmic contacts were subsequentry formed with alloyed Au/Ni/AuGe.

The 0.2μm-gate was then formed using our new gate fabrication process which is schematically shown in Fig. 2.

At first, a SiN film was deposited on a wafer and two different photoresists were successively coated on it. The upper photoresist was patterned by deep UV contact lithography to open a 0.5μm-stripe. A thin Al metal was then evaporated at an incident angle of 20°, which formed a 0.2μm-wide opening on the lower photoresist. After that, the lower photoresist was etched by O_2 RIE using the patterned Al film as a mask, and subsequently SiN was etched using SF_6 RIE.

Then, a stepped recess formation was carried out using Cl_2 RIBE and subsequent wet chemical etching. Chlorine ECR plasma was used for the inner recess formation with a gas pressure of 1.2×10^{-4}Torr to achieve an anisotropic etching and with an ion energy of 200V to reduce the etching damages [5]. The subsequent wet chemical etching formed the outer recess isotropically and also removed the residual etching damage completely.

At last, Al gate metal was evaporated and patterned by lift-off technique. The combination of the dry and wet etching formed a stepped recess structure whose inner recess was filled with the gate metal as shown in Fig. 2 .

In this process, the gate length can be reduced beyond the conventional photolithographic limit, since the gate length is determined precisely by the thickness of upper photoresist and the angle of Al evaporation. The source resistance of FET can also be reduced, especially enhancement mode one, because the outer recess region was thick enough to remain conductive. Figure 3 shows a cross-sectional SEM photograph after the gate metallization. The 0.2μm-gate formed in the inner recess is clearly seen in the photograph.

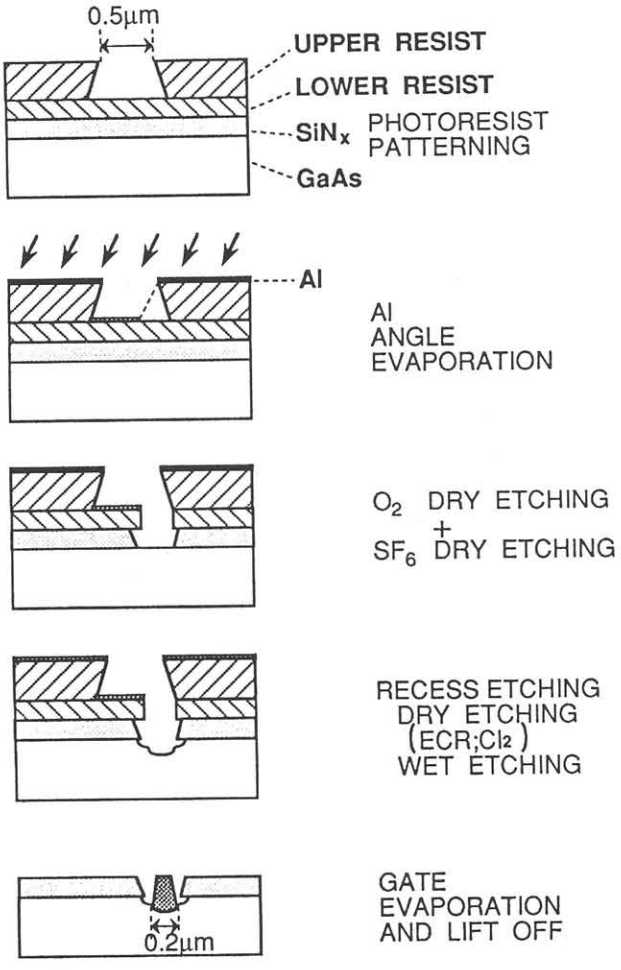

Fig.2 Fabrication flow of the 0.2μm-gate process.

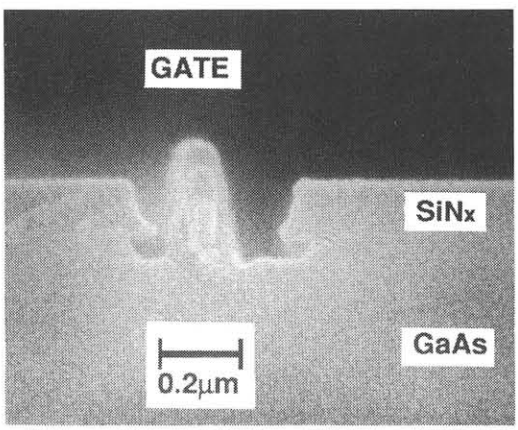

Fig.3 A cross-sectional SEM photograph of the 0.2μm-gate.

3. DC and RF performances

The I-V characteristics of the 0.2μm-gate BP-

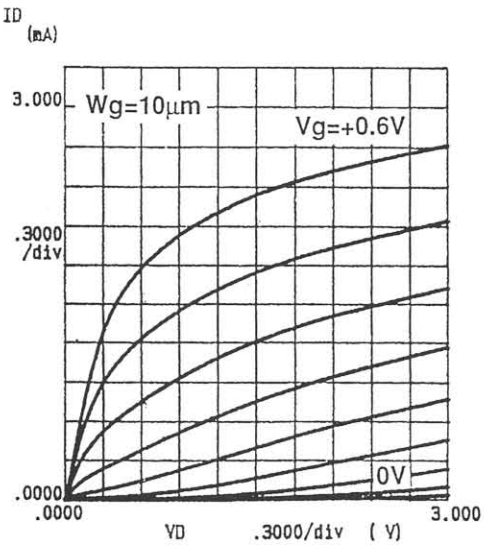

Fig.4 I-V characteristics of 0.2μm-gate BP-MESFET.

MESFET with threshold voltage (V_{th}) of 0V are shown in Fig. 4. The maximum transconductance (g_m) of 648mS/mm at a gate voltage (V_g) of 0.6V and K-value of 506mS/Vmm were obtained. To confirm the effectiveness of this fabrication process, the devices (stepped recess devices) were compared with the devices which have the same structure but the recess was formed only by the wet chemical etching (wet recess devices). Figure 5 shows the g_m's of the both types of devices at V_g=0.6V as a function of V_{th}. In the operating range of E-FET (V_{th}= 0V), the g_m's of the stepped recess devices are much larger than those of the wet recess devices, which is attributed to the small source resistance in the former devices.

S-parameter measurements were performed from 0.5 to 40GHz for the 150μm-wide devices. The short circuit current gain (h_{21}) was extracted from the S-parameters and the cut-off frequency (f_T) was determined by extrapolating h_{21} values to unity with a slope of -6dB/octave. Figure 6 shows h_{21} as a function of frequency for the stepped recess device. The f_T of as high as 96.1GHz is obtained.

4. Ring Oscillator

We have also fabricated the 19-stage E/D DCFL ring oscillators with the 0.2μm-gate BP-MESFETs.

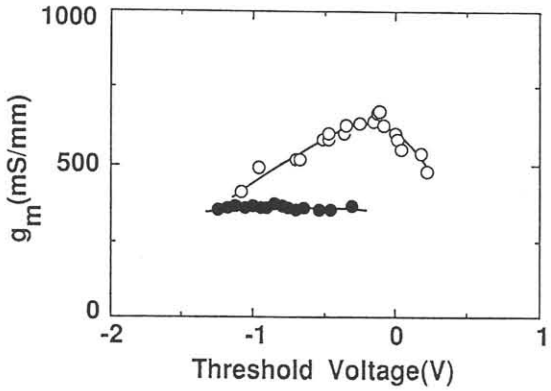

Fig.5 Transconductance as a function of threshold voltage. Open circles: stepped recess devices. Closed circles: wet recess devices.

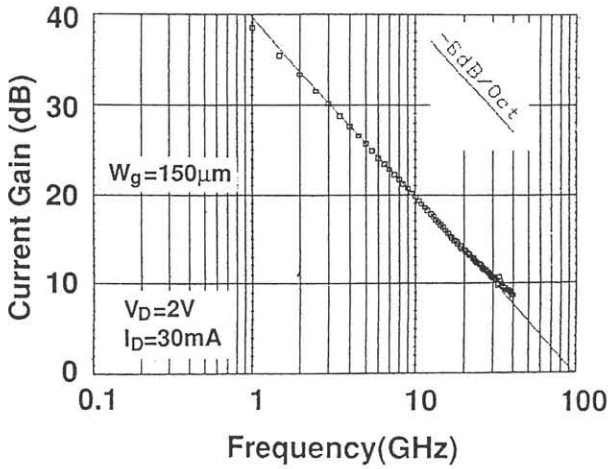

Fig.6 Frequency dependence of current gain h_{21} of 0.2μm-gate BP-MESFET.

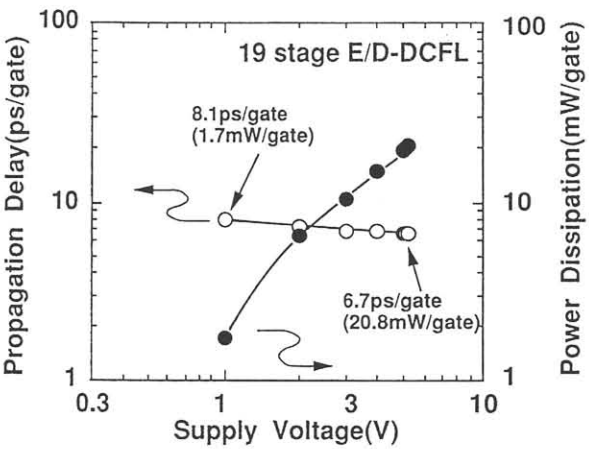

Fig.7 Propagation delay time and power dissipation as a function of supply voltage.

The gate length of load D-FET was 0.5μm. In Fig. 7, the propagation delay time (τ_{pd}) and power dissipation are shown as a function of supply voltage (V_{DD}). The τ_{pd} of 8.1ps/gate was obtained with a power dissipation of 1.7 mW/gate at V_{DD}=1V. To our knowledge, this is the best value ever reported for FET circuits at a low supply voltage condition (V_{DD}=1V). Furthermore, the τ_{pd} was reduced to 6.7ps/gate at V_{DD}=5.2V. The standard deviation of τ_{pd} across a 2-inch-diameter wafer was 0.38ps/gate, which indicates the good uniformity of this process.

5. Conclusions

We have demonstrated a new gate fabrication technique to realize a 0.2μm-gate. This technique can reduce the gate length shorter than the conventional photolithographic limit. The BP-MESFETs have been successfully fabricated using this technique which show high gm (648mS/mm) and high f_T (96.1GHz) due to the consequential lower source resistance. The E/D-DCFL ring oscillators with these devices showed excellent performances (τ_{pd} =6.7ps/gate at V_{DD}=5.2V and 8.1ps/gate at V_{DD}=1V). These results show that the 0.2μm-gate buried p-layer GaAs MESFETs fabricated by our new technique are suitable for the high speed and low power consumption digital ICs.

Acknowledgements

We would like to express our thanks to M. Sakuta and S. Takahashi for their encouragements during this work and also to K. Ohmuro for his valuable discussions.

References

(1) T. Ishibashi, O. Nakajima, K. Nagata, Y. Yamauchi, H. Ito, and T. Nittono, IEDM Tech. Dig., 826 (1988).

(2) Y. Yamauchi, O. Nakajima, K. Nagata, H. Ito, and T. Ishibashi, GaAs IC Symp. Tech. Dig., 121 (1989).

(3) J. F. Jensen, U. K. Mishra, A. S. Brown, L. G. Salmon, and M. J. Delaney, Microwave Journal, 32 (3), 131 (1989).

(4) M. Abe, T. Mimura, N. Kobayashi, M. Suzuki, M. Kosugi, M. Nakayama, K. Odani, and I. Hanyu, IEEE Trans. Electron Devices, 36 (10), 2223 (1989).

(5) G. L. Patton, J. H. Comfort, B. S. Meyerson, E. F. Crabbé, G. J. Scilla, E. de Frésart, J. M. C. Stork, J. Y. -C. Sun, D. L. Harame, and J. N. Burghartz, IEEE Electron Device Letters, 11 (4), 171 (1990).

(6) T. Saito, H. I. Fujishiro, T. Ichioka, K. Tanaka, S. Nishi, and Y. Sano, GaAs IC Symp. Tech. Dig., 117 (1989).

(7) M. Itoh, K. Ohmuro, H. Nakamura, S. Nishi, and S. Takahashi, Extended Abstracts 21st Conf. Solid State Devices and Materials, Tokyo, 285 (1989).