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Delay Times of 1/4-μm-Gate InAlAs-InGaAs HEMT's

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Abstract- InAlAs-InGaAs HEMT's with 0.22-μm-gate length have been fabricated and a maximum f_T of 132 GHz has been attained. Their delay times are decomposed into parasitic charging times, channel charging times, and transit times, and are quantitatively discussed. It is found that the saturated velocity of electrons in InGaAs is 2.7×10^7 cm/s, and the channel charging times of InGaAs HEMT's are much smaller by a factor of 4 ~ 9 than those of GaAs HEMT's with the same gate lengths.

1. Introduction

For several past years, high frequency and low noise performance of InP based InAlAs-InGaAs HEMT's have been demonstrated. U. K. Mishra *et al.* reported a 250-GHz cutoff frequency[1], and P. C. Chao *et al.* reported a 405-GHz maximum frequency of oscillation and a 0.3-dB noise figure at 18 GHz[2] using 0.15-μm-gate HEMT's. Thus, this material system is promising for high-speed, high-frequency, and low-noise devices.

Although these high performances are generally explained by high-sheet carrier density due to large InAlAs/InGaAs-conduction-band discontinuity and superior electron transport properties such as high mobility and high peak velocity, no quantitative analysis has been done yet. In this report, we decompose the total delay times into electron transit, channel charging, and parasitic charging times for fabricated InAlAs-InGaAs HEMT's with 1/4- to 1-μm gates for the first time, and quantitatively discuss the factors which dominate the delay times of HEMT's.

2. Material growth and device fabrication

The $In_{0.52}Al_{0.48}As$-$In_{0.53}Ga_{0.47}As$ modulation-doped heterostructure utilized in this study is shown in Fig. 1. The structure was grown by molecular beam epitaxy on Fe-doped semi-insulating (100) InP substrates at a temperature of 540 °C. The doping density for n^+-InAlAs was 4×10^{18} cm^{-3}. The undoped InAlAs layer between two highly doped InAlAs layers is to enhance the Schottky barrier of the gate metal. The upper n^+-InAlAs layer is designed to reduce the source and drain series resistance. The sheet resistance of the whole layers is 145 Ω/sq., and the carrier density and

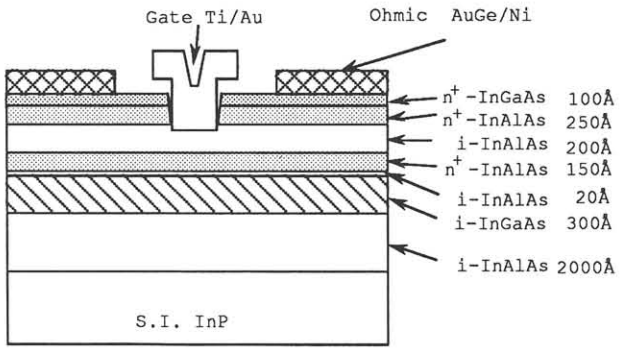

Fig. 1. HEMT structure.

mobility of the two dimensional electron gas under the gate metal were 3.0×10^{12} cm^{-2} and 9800 $cm^2V^{-1}s^{-1}$ at 300 K, respectively.

1/4-μm-gate devices with 50-μm-gate width were fabricated using electron beam lithography. Mushroom-shape-gate electrode was made by the lift-off method using tri-level resists composed of high molecular weight PMMA (top layer), low molecular weight PMMA (middle layer), and φ-MAC (bottom layer)[3]. AuGe/Ni was used for source and drain ohmic contacts with contact resistance of 0.14 Ω•mm. The gate region was recessed to a desired drain current by wet etching and metallized with Ti/Au. Moreover, 0.4- to 1-μm-gate devices with 150-μm-gate width were fabricated by conventional optical lithography on the same wafer.

3. Device performance

The typical source series resistance was estimated to be 0.30 Ω•mm from the results of TLM measurements. I-V characteristics of a 0.22 μm x 25 μm device are shown Fig. 2. The transconductance was about 400 mS/mm.

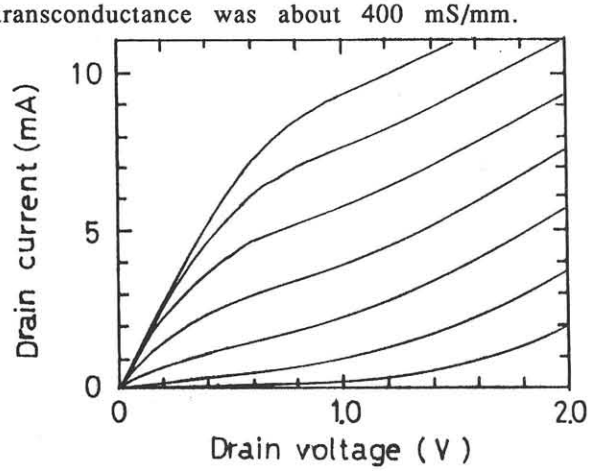

Fig. 2. I-V characteristics of HEMT with 0.22-μm-gate length and 25-μm-gate width. Gate voltage ranges from -1.2 to 0 V in 0.2-V increments.

Devices were characterized in the frequency region from 0.5 to 25.5 GHz on a Cascade RF probe station. The current gains, h_{21}, were extracted from the S-parameters and the unity current gain cutoff frequency, f_T, was calculated by extrapolating at 6 dB/octave. In order to subtract the effects of parasitics between device and probe heads, the reference plane of the S-parameter measurement was calibrated using fabricated open and short pads which were identical to the measured HEMT's except for the active region on the same wafer.

Figure 3 shows the frequency dependence of the current gain for a 0.22 μm x 50 μm device and an f_T of 132 GHz was obtained. The f_T's for the 0.5- and 1.0-μm-gate devices were 68, 35 GHz, respectively. These values are comparable to the best values reported for 1/4- to 1-μm-gate devices.

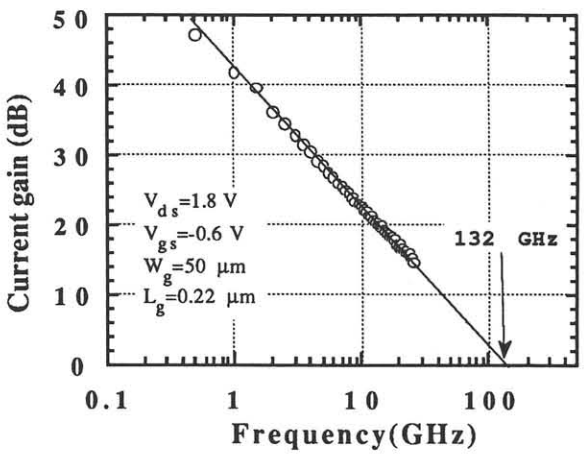

Fig. 3. Current gain versus frequency for 0.22-μm-gate HEMT.

4. Discussion

To discuss the intrinsic characteristics of devices, it is necessary to subtract the effect of parasitic elements, such as source and drain series resistances. Using an equivalent circuit model, total delay time (τ_{total}) can be represented as[4]

$$\tau_{total} = \frac{1}{2\pi f_T}$$

$$= \frac{C_{gs}+C_{gd}}{g_m}\left(1+\frac{R_s+R_d}{R_{ds}}\right) + C_{gd}(R_s+R_d) \quad (1)$$

$$= \tau_i + \tau_{s,d.} \quad (1)'$$

where, g_m is the intrinsic transconductance, C_{gs} is the capacitance between the gate and the

source, C_{gd} is the capacitance between the gate and the drain, and R_{ds} is the channel resistance. The second term of eq. (1) can be considered the parasitic charging time ($\tau_{s,d}$) for C_{gd} through R_s and R_d. The R_s+R_d and C_{gd} can be derived from the TLM measurement and the imaginary part of the Y_{12} parameter, respectively. This delay time was about 0.15 ps under the biases where f_T was maximized. Thus, the intrinsic delay time was estimated by subtracting $\tau_{s,d}$ from the total delay time.

The effective channel length and the channel charging time increase in importance as the gate length is shortened. The τ_i must be decomposed into the transit time of electrons ($\tau_{transit}$) and the channel charging time (τ_{cc}), i.e., $\tau_i = \tau_{transit} + \tau_{cc}$. These delay times can be divided using the drain-current dependence of the τ_i as reported by N. Moll *et al.*[5]. Figure 4 shows the relationship between the τ_i and the reciprocal of the drain current density for 1-, 0.5-, and 0.22-μm-gate-length devices. The $\tau_{transit}$ is the linearly extrapolated delay time at $W_g/I_d=0$ and the τ_{cc} was the difference between the τ_i and the $\tau_{transit}$.

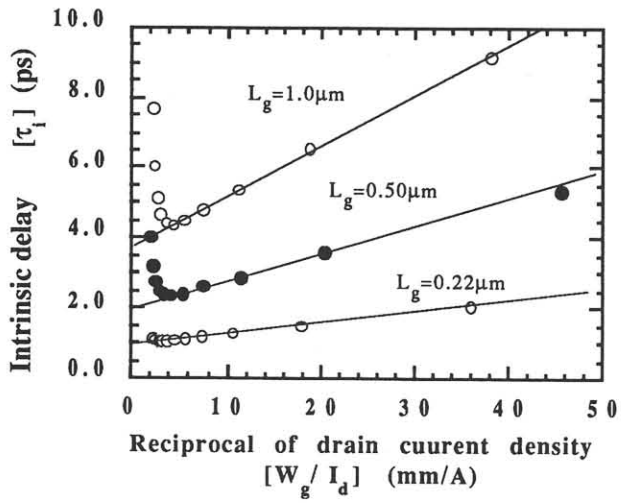

Fig. 4. Intrinsic delay time versus reciprocal of drain current density.

The relationship between electron transport and $\tau_{transit}$, which is defined above, can be represented as

$$\tau_{transit} = \frac{L_g+\Delta L}{v_s} \qquad (2)$$

where v_s is the saturated electron velocity and ΔL is considered the spread of the depletion layer at the source and drain end of the gate. Figure 5 shows the gate length dependences of the $\tau_{transit}$ and τ_{cc}. It is found that the $\tau_{transit}$ and τ_{cc} are proportional to gate length.

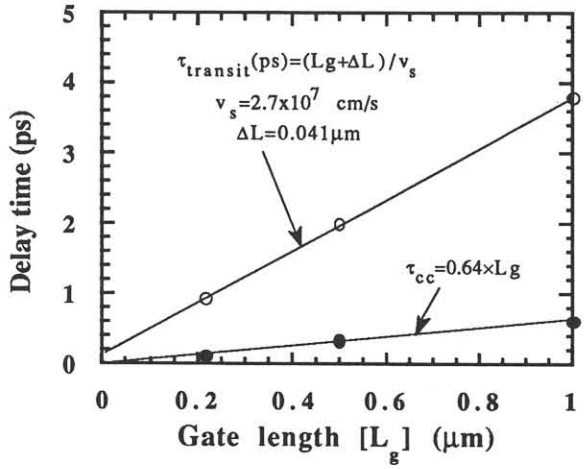

Fig. 5. Gate length dependence of delay times. open circles show transit times($\tau_{transit}$), and closed circles show channel charging times(τ_{cc}).

A ΔL is 0.041 μm and almost equal to the distance between gate metal and 2-DEG as expected. The linear relationship between $\tau_{transit}$ and L_g means the saturated velocity of electrons is a constant of 2.7×10^7 cm/s in this gate length region. This value is higher by a factor of 1.5 than the drift velocity of electrons under the electric field strength of 12 kV/cm in InGaAs measured by the time-of-flight[6]. This result suggests the presence of the velocity overshoot effect in HEMT's with gate lengths below 1.0 μm. Moreover, this v_s of InGaAs is higher than that of GaAs[5,7] by a facto of 1.2 ~1.4. However, the v_s is constant for 1/4- to 1-μm-gate devices, contrary to our expectation. Further study and controlled experiments on shorter gate devices must be performed to utilize the velocity-overshoot effect.

Table I summarizes these delay times under the biases where f_T's are maximized, and compares them with the delay times for an AlGaAs/GaAs (GaAs), and $Al_{0.25}Ga_{0.75}As$/ $In_{0.25}Ga_{0.75}As$ (pseudomorphic) HEMT's obtained by N. Moll *et al.*[5]. In their paper, it was pointed out that the channel charging time of pseudomorphic HEMT is smaller than that of GaAs HEMT, and they explained it as resulting in large part from the relatively large electron density[5]. We found that the reduction of channel charging time of the InP-based InGaAs HEMT is more conspicuous than the others. The fraction of the channel charging time in the total delay time is only 9%, and much smaller than the times of pseudomorphic and GaAs HEMT's by factor of 2.7 and 4.0, respectively. According to ref. 8, τ_{cc} can be considered as the charging time by the drain current for the additional channel charge necessitated by nonconstant electron velocities, and can be related to the low field mobility of electrons. So, this advance is attributed to material characteristics such as the high mobility and sheet carrier density of electrons.

Table I. Summary of delay times of HEMT's.

	InP-base HEMT's (this work)			Pseudo-morphic HEMT[5]	GaAs HEMT[5]
L_g (μm)	1.0	0.50	0.22	0.15 ~0.25	
f_T (GHz)	35	64	132	98	64
τ_{total} (ps)	4.5	2.5	1.2	1.6	2.5
$\tau_{s,d}$ (ps)	0.15	0.13	0.15	---	---
τ_{cc} (ps)	0.62	0.34	0.11	0.4	0.9
$\tau_{transit}$ (ps)	3.8	2.0	0.94	1.2*	1.6*

* These $\tau_{transit}$'s consist of the electron transit time to across the L_g and the delay time required for electrons to drift across the drain depletion region.

V. Conclusions

InP-based InAlAs-InGaAs HEMT's with 1/4- to 1-μm-gate lengths have been fabricated. The devices with 0.22-, 0.50-, and 1.0-μm-gate lengths show high f_T's of 132, 64, and 35 GHz, respectively. Their delay times have been decomposed into parasitic charging, channel charging, and electron transit times. It has been clarified that the total delay times of 1.2 ps, corresponding to an f_T of 132 GHz, consists of $\tau_{s,d}$ = 0.15 ps, τ_{cc} = 0.11 ps, and $\tau_{transit}$ = 0.94 ps. The saturated velocity is 2.7×10^7 cm/s and is constant from the 1/4- to 1-μm-gate length region and is higher than that of GaAs by a factor of 1.2 ~1.4. The fraction of the channel charging time in the total delay time is only 9% for a 0.22-μm-gate HEMT. This is very small when compared with the same size-gate-GaAs HEMT's. This advance can be attributed to the high mobility and sheet carrier density of electrons.

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