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Improvement of GaAs MESFET's Characteristics on SiO_2-Back-Coated Si Substrate by MOCVD

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We show that use of SiO_2 back-coated Si substrate is effective to obtain a low background electron concentration in an undoped GaAs layer grown on Si, particularly at high temperature, by MOCVD. Higher growth temperature improves crystallinity of the GaAs layer grown on Si and helps to suppress the sidegating effect of GaAs MESFET's fabricated on Si. A low background electron concentration in the undoped GaAs layer is required for good pinch-off of the MESFET's. By using SiO_2 back-coated Si substrate, the undoped GaAs with an electron concentration as low as $1x10^{15}$ cm^{-3} was grown even at 750 °C. The maximum transconductance of 160 mS/mm, good pinch-off and suppressed sidegating were achieved for the MESFET on SiO_2 back-coated Si.

1. INTRODUCTION

There has been a growing interest in growth of GaAs on Si substrates (GaAs/Si). Although serious problems inherent in growth of GaAs/Si are mismatch of lattice parameter, thermal expansion coefficient and unintentional Si autodoping in the grown GaAs layer, laser diodes, metal-semiconductor field-effect transistors (MESFET's) and high electron mobility transistors (HEMT's) have been fabricated on Si using the molecular beam epitaxy (MBE) or the metalorganic chemical vapor deposition (MOCVD) technique.[1-5] GaAs MESFET's on Si with the improved pinch-off characteristic and the suppressed sidegating effect are necessary to produce GaAs IC's on Si. In general, undoped layers grown on Si by MOCVD show n-type conductivity. The unintentional autodoping affects the pinch-off characteristics of GaAs MESFET's and HEMT's grown on Si. To ease this problem some doped GaAs buffer layers with vanadium,[3] and some lowered growth temperature to increase resistivity of undoped GaAs layer.[4] Not much attention has been paid on the sidegating effect, which is an extremely undesirable effect in the GaAs IC's. In this paper, we show that use of SiO_2 back-coated Si substrate is effective to obtain an undoped GaAs layer grown on Si particularly at high temperature by MOCVD. The undoped GaAs layer with a low electron concentration grown on Si at high temperature by MOCVD improves pinch-off and suppresses sidegating of a GaAs MESFET fabricated on Si.

2. EPITAXIAL GROWTH AND DEVICE FABRICATION

All epitaxial layers were grown on (100) Si substrates oriented 2 ° off toward [011] in an RF-heated horizontal MOCVD reactor at atmospheric pressure using the two-step growth technique. Before the epitaxial growth, 720 nm-thick SiO_2 films were sputtered on the back side of Si

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substrates. The source materials were trimethylgallium (TMG), trimethylaluminum (TMA), arsine (AsH_3) and phosphine (PH_3). To study the unintentional Si autodoping, 4 μm-thick undoped GaAs layers were grown at 750 °C on n-Si substrates with and without SiO_2 back-coating. The carrier concentration was measured by the electrochemical capacitance-voltage (C-V) measurement. Prior to the growth, Si substrates were heated at 1000 °C for 10 min in the mixture of AsH_3 and H_2 ambient in order to remove the oxide. For MESFET's, the following layers were successively grown on p-Si substrates with and without SiO_2 back-coating: a 125 Å-thick GaAs nucleation layer at 400 °C, a 0.8 μm-thick undoped GaAs buffer layer at 700 °C, a 1 μm-thick p-$Al_{0.3}Ga_{0.7}As$ layer at 700 °C, a 1 μm-thick undoped GaAs layer at various temperatures from 650 to 750 °C, a 0.3 μm-thick channel layer doped with Se to $3x10^{17}$ cm^{-3} at 750 °C and a 600 Å-thick ohmic contact layer doped with Se to $1x10^{18}$ cm^{-3} at 750 °C. Then, MESFET's were fabricated using the standard GaAs processing technique. A 0.1 μm-thick SiO_2 film was sputtered on the n^+-GaAs layer, and a 0.8 μm-deep mesa isolation was performed by chemical etching. AuGe/Ni/Au source and drain ohmic contacts were formed by evaporation/liftoff and alloyed at 380 °C for 1 min in flowing N_2 gas. The gate region was recessed to the depth of about 0.2 μm by chemical etching, and the gate contact was made by evaporation/liftoff of Ti/Au. A schematic cross section of the fabricated MESFET structure on the GaAs/Si is shown in Fig. 1. The test pattern consisting of two 80 μm-long ohmic contacts to the n^+-GaAs layer regions separated by 8 μm with the etched isolation was used to evaluate the device isolation.

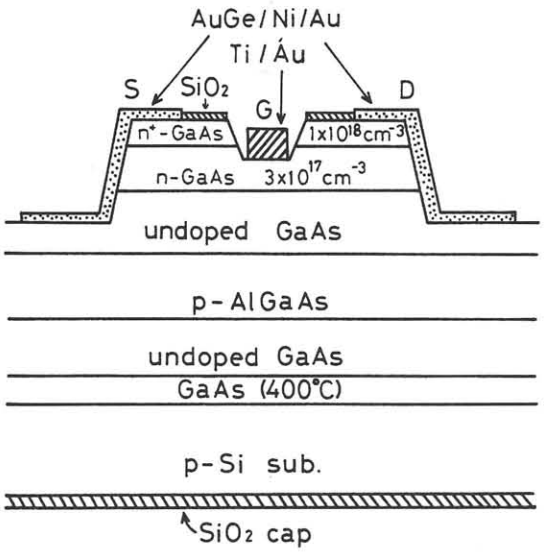

Fig. 1. Structure of GaAs MESFET on SiO_2 back-coated Si substrate.

3. RESULTS AND DISCUSSIONS

Figure 2 shows the electron concentration profiles of the undoped GaAs layers grown at 750 °C on Si substrates with and without SiO_2 back-coating. The electron concentration of $1x10^{17}$ cm^{-3} is obtained for the GaAs/Si without SiO_2 back-coating, but the electron concentration decreases with increasing the SiO_2 thickness. The electron concentration of the GaAs/Si with SiO_2 back-coating thicker than 480 nm is as low as $1x10^{15}$ cm^{-3}, which indicates that the SiO_2 back-coating prevents transport of Si atoms to the growing GaAs surface in gas phase. The secondary ion mass spectroscopy measurement supports the above result.[6)]

The isolation leakage current in the undoped GaAs layers measured at 0.1 V is summarized in Table I. Without SiO_2 back-coating, the isolation leakage current increases from 4 nA to 1900 μA with increasing the growth temperature of 650 to 750 °C. With SiO_2 back-coating, on the other hand, it remains less than 4 μA even

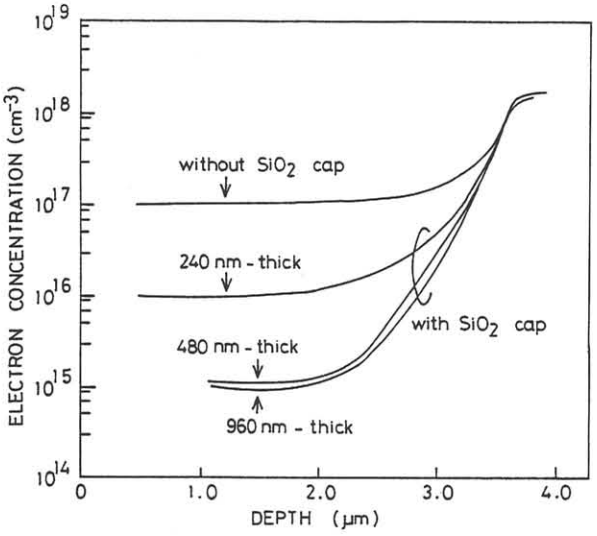

Fig. 2. Electron concentration profiles of the undoped GaAs layers grown at 750 °C on Si substrates with and without SiO_2 back-coating.

Table I. Isolation leakage current in the undoped GaAs layers grown at 650, 700 and 750 °C on Si substrates with and without SiO_2 back-coating. The thickness of SiO_2 back-coating is 720 nm.

T_g (°C) \ SiO_2 cap	without SiO_2 cap	with SiO_2 cap
650	4×10^{-3}	3×10^{-3}
700	4-1860	3×10^{-3}
750	460-1900	4

(μA)

when the growth temperature is 750 °C. The transmission line model measurements indicate that the p-AlGaAs buffer layer is necessary to prevent the current flow from reaching the GaAs/Si interface.[7] These results imply that if MESFET's are grown at 650 °C on Si, MESFET's should have good pinch-off characteristics even without SiO_2 back-coating. As will be discussed later, however, higher growth temperature is required to suppress the sidegating effect.

The relationship between the gate bias and the square root of source-drain current of MESFET's on Si substrates with and without SiO_2 back-coating is shown in Fig. 3. The undoped GaAs layers beneath the channel layers were grown at 700 °C. The MESFET on Si substrate without SiO_2 back-coating has a serious problem with pinch-off because of the lateral current flow in the undoped GaAs layer beneath the channel layer. The maximum transconductance (g_{mmax}) and the K-value are 74 mS/mm and 9.6 mA/V^2mm, respectively, for the MESFET with a 2.2x15 μm gate. However, the MESFET on SiO_2 back-coated Si substrate shows a better pinch-off characteristic and a higher K-value. For the MESFET with a 2.5x15 μm gate, the g_{mmax} and the K-value are 160 mS/mm and 46.8 mA/V^2mm, respectively. The reason for the higher K-value is that the current flow in the undoped GaAs layer beneath the channel layer is suppressed by using SiO_2 back-coated Si substrate.

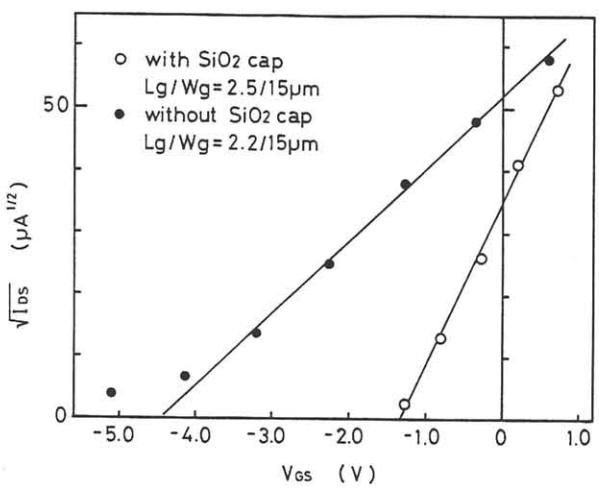

Fig. 3. Relationship between the gate bias and the square root of the source-drain current of MESFET's on Si with and without SiO_2 back-coating.

Figure 4 is the normalized drain saturation current as a function of the side gate bias (V_{sg}) for the MESFET's on SiO_2 back-coated Si substrates. The growth temperature of the undoped GaAs layer beneath the channel layer are 650, 700 and 750 °C. The values are normalized to their values at V_{sg}=0 V. The sidegating pad is located 30 μm away from the source of the device. The sidegating effect is reduced by increasing growth temperature of the undoped GaAs layer beneath the channel layer. The reduction of drain saturation current for the growth temperature of 750 °C is less than a 5 % even when -10 V is applied to a pad located 30 μm away from the source.

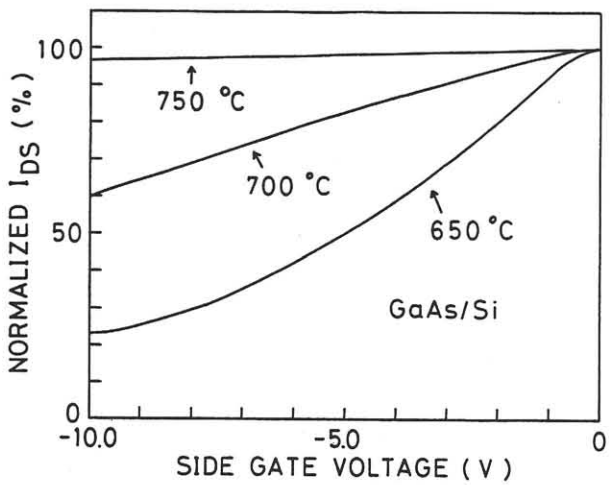

Fig. 4. Comparison of the sidegating effect of MESFET's on SiO_2 back-coated Si substrates for various growth temperatures of the undoped GaAs layers.

4. CONCLUSIONS

We have shown that SiO_2 back-coating of Si substrate is effective to obtain a lower background electron concentration in MOCVD-grown undoped GaAs layer on Si, and the pinch-off and the sidegating effect characteristics of GaAs MESFET's on Si are improved by using combination of SiO_2 back-coated Si substrate and increasing of growth temperature.

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