Shallow p⁺-n Junction Formation by As⁺-Preamorphization and Field-Retarded Diffusion

Sang-Jik Kwon, Hyeong-Joon Kim, and Jong-Duk Lee Inter-University Semiconductor Research Center, Seoul National University, Shinlim-Dong, Gwanak-Gu, Seoul 151-742, KOREA

The effects of preamorphization by As^+ implantation have been investigated in this study. The compensation of carriers and field-retarded diffusion of boron ions due to implanted As^+ were observed in both the experiment and the computer simulation by PREDICT program. The shallow p^+ -n junction, of which an effective junction depth was less than 0.11 μ m, was formed with low leakage current density through optimizing the thickness of the preamorphized layer.

1. Introduction

The formation of shallow source/drain junctions is one of the major requirements for the scaled CMOS technologies. CMOS requires n^+ -p and p^+ -n junctions for the formation of both NMOS and PMOS source/drain region. Shallow n^+ -p junctions can be easily formed by arsenic ion implantation. However, the formation of shallow p^+ -n junctions is much difficult in spite of the low energy boron implantation because of the channeling phenomenon of boron atoms.^{1,2}

One way to eliminate boron channeling is to preamorphize the silicon substrate prior to the boron implantation. Several papers have reported that the preamorphization method can eliminate completely boron channeling.³⁻⁷

In this work, we investigated the effects of preamorphization by As⁺ implant on the boron profile. The advantages for selecting arsenic ion as an element for the preamorphization of silicon substrate are those that As⁺ ions can be easily available in an existing implanter system without any modification and easily amorphize silicon substrate because of its high mass. Also, the internal electric field produced by arsenic dopants during annealing can retard significantly the boron diffusion.^{8,9} In addition, the effective junction depth by electrical

carriers can be shorter than the depth by atomic borons due to compensation effect in the tail region.

2. Experiment

Samples used for the experiments were 4-inch diameter n-type Si wafers of (100) orientation and $10 \sim 15 \Omega$ -cm resistivity. All wafers were cleaned and etched in a 10:1 HF solution to remove screen oxide. Implantation was carried out on a Varian CF-3000 scanning-beam implanter system. During the implantation, a wafer on the platen was cooled down by water in order to reduce beam heating. All wafers were implanted at a tilt angle of 7°. In order to preamorphize the silicon substrate and obtain an optimum preamorphization condition, arsenic ion implantation was performed at a dose level of 4x10¹⁴ cm ⁻² larger than the critical dose for amorphizing the silicon substrate and at energies ranging from 40 keV to 100 keV. A subsequent boron implantation was carried out with the energy of 10 keV at a dose of 1.5x10¹⁵ cm⁻². The wafers were annealed at 550°C for 30 min in nitrogen ambient prior to the high temperature anneal. Then, the rapid thermal annealing (RTA) was carried out at 1050 °C for 10 sec in nitrogen ambient in order both to activate dopants and to remove residual defects. The profiles of B, As, and electrical carriers were obtained using

secondary ion mass spectrometry (SIMS) and spreading resistance profile (SRP) measurements. Diodes and PMOS transistors were fabricated to evaluate junction leakage and drain *I-V* characteristics.

3. Results and Discussion

3.1 Depth profiles

Fig.1 shows the SIMS depth profiles of boron, which was implanted with an energy of 10 keV and a dose of 1.5×10^{15} cm⁻² into As⁺ preamorphized samples and a nonpreamorphized single crystalline silicon. In SIMS analysis, primary oxygen ion beam was used to enhance the sensitivity for boron atoms. The primary ion energy was 5 keV and the incidence angle was 60° from the normal direction of a sample. The as-implanted boron profiles show that ion channeling can be reduced by As⁺ preamorphized layer.

Channeling is reduced as the energy of arsenic implantation for preamorphization increases and completely eliminated in the samples preamorphized with 80 keV and 100 keV. SIMS profiles of boron in the samples annealed at 550°C for 30 min and subsequently at 1050°C for 10 sec in nitrogen ambients are shown in Fig.2. It is well known that enhanced or retarded diffusion due to the internal electric field created by the impurity dopants.^{8,10} In this experiment, the internal electric field is formed by the space charge between positively charged arsenic ions and electrons during annealing. The resulting inward electric field enhances in-diffusion of As^+ but retards in-diffusion of B⁻ ions. Consequently, the redistribution of boron during annealing is suppressed by the presence of arsenic ions. Thus, the boron profiles in the preamorphized and annealed samples would result in shallower junctions than those in the samples preamorphized by using other elements, such as Si or Ge.

The calculated profile of boron implanted into preamorphized silicon could be obtained from the computer simulation by PREDICT program. The calculated boron profiles in the samples preamorphized by As or Ge implantation with the energy of 60 keV are shown in Fig.3. As-implanted boron profiles are the same for As^+ -and Ge^+ -preamorphized samples, but in the case of annealed profiles, the boron profile in the As^+ -preamorphized sample is much shallower than that in the Ge^+ -preamorphized sample.



Fig. 1 SIMS depth profiles of B atom for samples preamorphized with various As implant energies.



Fig. 2 SIMS depth profiles of B atom for samples preamorphized and annealed at 950°C for 30 min and at 1050°C for 10 sec.



Fig. 3 Depth profiles of B atom calculated for both As and Ge preamorphized samples by the computer simulation with PREDICT program. Preamorphization energy was all 60 keV.

This result is associated with the field-retarded diffusion of boron ions due to the electric field created by arsenic ions. The effect of retarded diffusion is also appeared in this experiment. As shown in Fig.1 and Fig.2, it is noticeable that the difference of profile depths between as-implanted profile and annealed profile of B atom becomes to be smaller as the peak position of arsenic concentration approaches to the boron tail region, and it is greatest for the non-preamorphized sample. For the cases of 60, 80, and 100 keV As⁺ implants, the boron depths of the as-implanted samples in the tail region are almost the same but different for the annealed samples.

Another factor that makes the effective p^- -n junction depth shallower is the compensation of p-type carriers by As⁺ dopant in the B tail region. Fig.4 shows both the SIMS depth profiles of As and B, and electrical carrier profile by SRP for the sample, which was preamorphized with 60 keV As and subsequently annealed. The depth at which arsenic concentration coincides with boron concentration is about 0.11 μ m, corresponding to the concentration of 1.5×10^{18} cm⁻³. Thus, the effective p⁺-n junction formed by electrical carrier is reduced a little bit as compared with the depth by atomic boron.



Fig. 4 (1) SIMS depth profile of B atom, (2) electrical carrier profile obtained by spreading resistance profiler, and (3) SIMS depth profile of As atom for sample preamorphized with 60 keV As⁺ implant energy and annealed at 1050° C for 10 sec.

3.2 Diode and PMOS transistor characteristics

Dislocation-like residual defects remained after RTA become the source of junction leakage current, but the leakage current level depends on the position of these defects relative to a p^+ -n junction interface.⁴

Channeling is more suppressed as the thickness of preamorphized layer increases, but leakage current excessively increases with increasing the thickness more than the critical value.

Fig.5 shows the leakage current characteristics of reverse-biased p^+ -n diodes. The leakage current levels in the samples preamorphized with the As⁺ energies of 40 and 60 keV are almost the same as that in the non-preamorphized sample, but excessively increases in the samples preamorphized with the energies higher than 80 keV. The level of leakage current increases as the distance of p^+ -n junction away from the amorphous/crystal (a/c) interface decreases. Fig.6 shows the *I-V* characteristics for



Fig. 5 *I-V* characteristics of PMOSFET (W/L=20/1 μ m), of which preamorphized layer was obtained with As⁺ / 60 keV.



Fig. 6 *I-V* characteristics of reverse-biased p^+ -n diode as a function of As⁺ implant energy for preamorphization.

PMOSFET with the gate length of 1.0 μ m and the width of 20 μ m with the preamorphization condition of As⁺ / 60 keV. The *I-V* characteristics for the preamorphized sample show similar properties with those for nonpreamorphized sample, but become to be deteriorated considerably for the As⁺ energies higher than 80 keV. It seems to be due to the excessive junction leakage current.

4. Conclusions

The channeling effect of implanted boron atoms can be completely eliminated through preamorphization by As⁺ implant. Owing to the compensation of carriers and field retarded diffusion of boron ions by arsenic ions in the tail of boron profile, p^+ -n junction with an effective depth of about 0.11 µm was obtained in the implantation conditions of As⁺ / 60 keV / 4x10¹⁴ cm⁻² and B⁺ / 10 keV / 1.5x10¹⁵ cm⁻² followed by furnace anneal at 550° C for 30 min and subsequent RTA at 1050°C for 10 sec. Leakage current density of the resulting p⁺-n diode was comparable to that in non-preamorphized sample, and PMOSFET transistor characteristics were also stable.

ACKNOWLEDGMENT

The authors thank Mr. Y.M.Park for his help in SIMS analysis, and Mr. C.S.Kim for his aids in RTA process. The authors also would like to thank prof. K.S.Seo for his grateful discussion.

REFERENCES

- T. M. Lin and W. G. Oldham: *IEEE Electron Device* Lett. EDL-4 (1983) 59.
- T. M. Lin and W. G. Oldham: *IEEE Electron Device* Lett. EDL-5 (1984) 299.
- B. Y. Tsaur and C. H. Anderson, Jr.: J. Appl. Phys. 54 (1983) 6336.
- H. Ishwara and S. Horita: Japanese Journal of Applied Physics. 24 (1985) 568.
- M. Delfino, D. K. Sadana, and A. E. Morgan: *Appl. Phys. Lett.* 49 (1986) 575.
- M. C. Ozturk, J. J. Wortman, C. M. Osburn, A. Ajmera, G. A. Rozgonyi, E. Frey, W. Chu, and C. Lee: *IEEE Trnas. on Electron Devices.* 35 (1988) 659.
- C.P.WU, J.T.McGinn and L.I.Hewitt: Journal of Electronic Materials. 18 (1989) 721.
- R. B. Fair, J. J. Wortman, J. Liu, M. Tischler, and M. A. Masnari: *IEEE Trans. on Electron Devices*. ED-31 (1984) 1180.
- T. K. Okada and K. Kato: Extended Abstracts of the 21th Conference on Solid State Device and Materials. Tokyo (1989) 165.
- S. K. Ghandhi: VLSI Fabrication Principles. New York:Wiely (1983) 121.