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Transient RTA of Low-Dose High Energy Phosphorus Implanted Silicon

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A novel ramped RTA technique is proposed for efficient low thermal budget post-implantation annealing of low-dose high energy P-implanted silicon wafers. Results obtained with this short effective annealing time of 300ms on 3" substrates proved quite convincing in comparison with conventional furnace anneal performance. Full activation, minimum profile motion and generation rates below $0.3mA/cm^3$ could be achieved in the subsurface region, which is of interest for device applications. Inhomogeneity of the sheet resistivity due to transient temperature gradients across the wafer remained at 2%, comparable to or lower than in furnace annealed samples.

INTRODUCTION

Low and moderate dose (10^{13}-$10^{14}cm^{-2}$) ion-implantation using MeV energies is becoming increasingly important in advanced IC technology for the formation of buried conductive layers [e.g.1]. In many applications phosphorus is preferred to arsenic due to the larger achievable projected ranges.

The post-implantation anneal step has the combined role of electrical dopant activation by moving the dopant atoms into substitutional lattice sites, and elimination of primary ion-induced defects formed during implantation. During damage anneal the primary defects interact with the implanted dopants, which leads to point-defect enhanced diffusion. This is especially critical in the case of boron but also phosphorus profiles are prone to this adverse effect [2]. Therefore in any damage anneal step the primary defects have to be first eliminated. The competing thermally activated processes involve largely different activation energies, whereby the highest of about 5eV is just the one of Si self-diffusion required to excess point defect removal. Sedgwick [3] suggested to use the inherent selectivity of RTA in post-implant annealing to suppress the undesired dopant motion processes. Yet, even in the usual isothermal RTA temperature-time domain a significant profile broadening owing to the practical limits could not be prevented.

The remaining point defects usually form extended secondary ones, mostly dislocations which can coalesce and climb to interfaces or remain in form of dislocation loops close to the projected range of the implanted profile, as revealed by TEM for doses above a critical minimum. According to Tamura et al. [4] this is, independent of the kind of implanted species just $2 \cdot 10^{13}$-$1 \cdot 10^{14}cm^{-2}$. Also recent high resolution X-Ray Diffraction studies indicate a resolution limit in this order, but the minimum visible strain here depends on the kind of dopant atoms used [5].

THE RAMPED RTA TECHNIQUE

In this work we made use of the fast, controllable ramping capability of the Peak Systems LXU 35 lamp-heating system by employing the ramped RTA technique, a kind of transient annealing method. The peak temperature for the ramped anneals was selected in a way that allowed considerable Si self-diffusion. The set peak temperature was reached in 3 seconds by closed loop control and the ramp down to 500°C was completed in 7 seconds. Thereafter the lamp was switchedoff, and the wafer cooled down to room temperature. In order to derive an effective duration in the ideal T vs. t profile approximation for our T-RTA cycles we used the method described in [6]. Ramp-up rates of 250-350 K/s and ramp-down rates of 60-120 K/s resulted in the effective durations of 350-250ms for the peak temperatures between 1200-1600K, respectively. The obtained T-RTA treatments are therefore considered to be roughly isochronal with t_{eff}=300ms.

The very fast thermal transients, we use in the experiments, could have detrimental effects on the device characteristics. Temperature gradients developed across the wafer during the thermal process may cause nonuniform process results and even the formation of dislocation arrays, slip dislocations. These effects had to be studied in detail.

EXPERIMENTAL

High resistivity, 6-10 Ωcm (100) 3" silicon wafers have been used in the experiment. One half of every wafer was patterned containing different size Van der Pauw and aluminum gate MOS capacitor structures. They were formed with the low-dose implanted layers using deep plug-diffusion surface contacts for the electrical evaluation of the crystal quality. The other half was subjected to profiling studies. The screen oxide layer of 800Å for the MeV ion-implantation was later used as gate dielectric under the aluminum electrodes. As the high energy implantation immediately preceded the damage anneal step, no other contribution influencing the final crystal quality is expected from the processing.

The 1.5 MeV P implantation was done at room temperature, the low dose of $5 \cdot 10^{13}cm^{-2}$ excluded the possibility of amorphization. Ion-beam annealing during implantation was also prevented by the low average ion-beam current density of $<0.1\mu A/cm^2$.

The N_2 furnace anneal steps were performed at 1200 and 1300K for 30 min. Time temperature profiles of the T-RTA steps in N_2 are shown below.

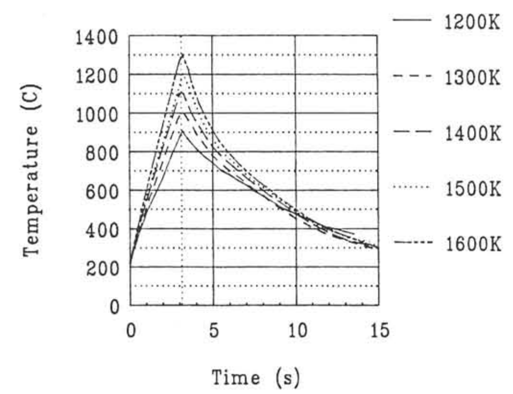

Fig. 1 Temperature vs. time profiles used in the "isochronal" 300ms T-RTA steps.

RESULTS AND EVALUATION

With the fast ramp rates up to 350K/s no formation of slip lines or other kind of plastic deformation could be observed even at the highest set peak temperature of 1500K.

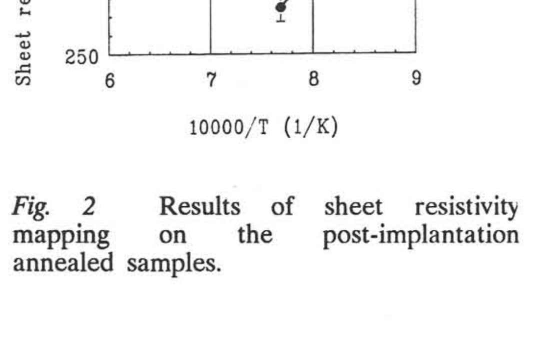

Fig. 2 Results of sheet resistivity mapping on the post-implantation annealed samples.

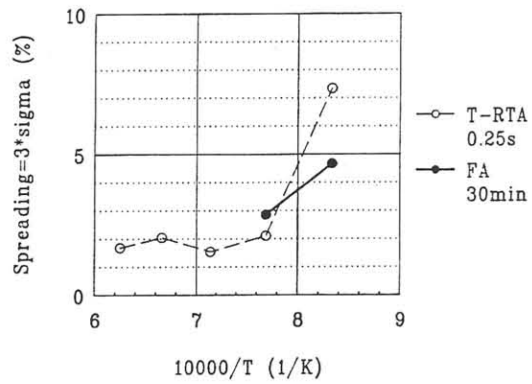

Fig. 3 Spr e ading of the sheet resistivity values across the wafers (3σ) expressed in % of the mean values, respectively, as a measure of process uniformity.

Typical results of the sheet resistivity mapping on the Van der Pauw structures are shown in Fig.2. The high R_S values obtained for the 1200K anneals reflect a lack of activation, whereas the full dose seems to be activated above 1300K with both, T-RTA and furnace anneal. Also the 3σ error bars in the R_S data indicate this behavior. Fig.3 reflects the high degree of uniformity across the T-RTA wafers, the R_S spreading remains below 2% for the completely activated cases.

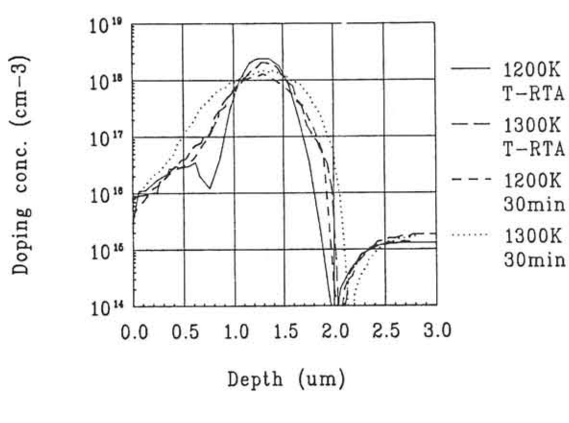

Fig. 4 Spreading resistance carrier concentration profiles of 1.5 MeV, $5 \cdot 10^{13} cm^{-2}$ P-implanted samples after 1200K and 1300K T-RTA and furnace post-implantation anneal.

It is obvious from the carrier depth profiles that at 1300K and above a complete activation of the implanted dose occures. The anomalously low carrier concentration values in the profiles of T=1200K samples indicate mobility reduction by defects. The carrier concentration depth profiles of all the other T-RTA samples not shown here almost coincide, which is a sign of a minimum dopant motion.

Zerbst analysis has been used for the electrical evaluation of the crystalline quality on the MOS capacitors formed on top of the high energy implanted regions. The present structure offers a unique chance for simple deduction of generation lifetime and velocity vs. depth profiles by the C-t measurement. Since the carrier concentration increases with depth, the electric field can penetrate the subsurface region. Increasing the reverse bias the measured, decreasing lifetime values will reflect the effect of centers lying in a depth defined by the depletion layer increment obtained from the C-V doping profiling. In a first approximation we computed the generation parameter with the doping concentration corresponding to that depth. Hereby the method underestimates the value of the actual lifetimes in the roughly exponentially increasing doping profiles.

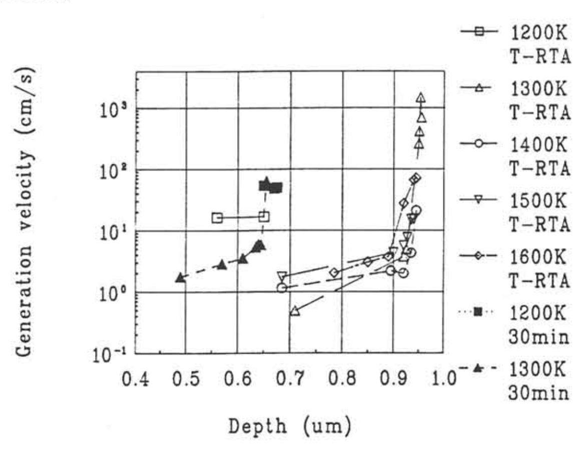

Fig.5 Generation velocity vs. depth profiles obtained from the Zerbst C-t analysis of the differently annealed samples

In Fig.5 the extreme high generation velocity values obtained on the T=1200K samples, even at relatively shallow depth reflect the imperfect damage anneal. Also the T=1300K furnace annealed sample showed an inferior performance as a result of the excessive out-diffusion compared to the T-RTA samples of more or less equal characteristics.

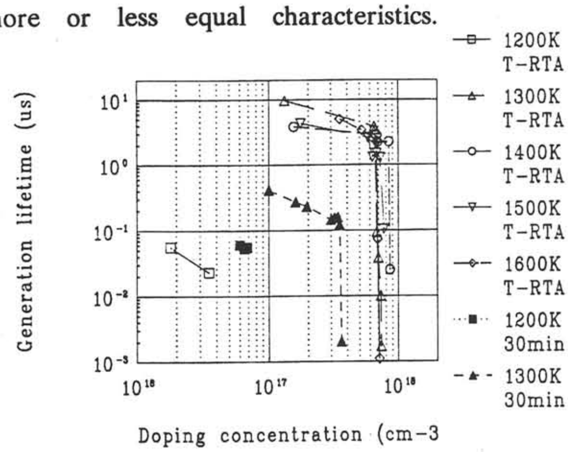

Fig.6 Generation lifetime vs. carrier concentration plots for all the samples derived from the Zerbst results.

In this comparison the superiority of T-RTA is even more evident. The insignificant differences obtained between the individual lamp-annealed specimen are within the measurement accuracy. All of the T-RTA samples have lifetimes of at least one and a half orders of magnitude longer than the furnace annealed one at a given concentration in Fig.6.

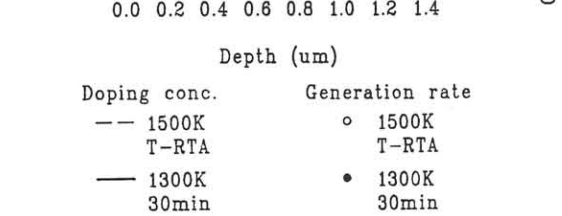

Fig.7 Carrier concentration vs. depth profiles of the selected 1500K T-RTA and the 1300K furnace annealed samples in the subsurface region along with calculated generation rate data.

Finally in Fig.7 we plotted the results we believe demonstrate the benefits of the proposed technique in this particular application. The selected 1500K T-RTA post-implant anneal not only suppressed the doping profile motion, but also caused an effective reduction of generation/recombination centers associated with extended defects in the active region compared to the conventional method. The obtained low generation rates also favorably compare with published literature data [7].

SUMMARY AND CONCLUSIONS

The proposed novel transient RTA technique can perform the complete dopant activation with effectively suppressing the motion of the high energy implanted low-dose phosphorus profile. The 300ms T-RTA damage anneal step at T_{peak} > 1300K provided generation rates of more than an order of magnitude below those in the furnace annealed reference sample. This low thermal budget step can easily be integrated in any processing sequence and offers a very promising way for the fabrication of efficient high energy implanted buried injectors in EEPROM structures [1].

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