Extended Abstracts of the 22nd (1990 International) Conference on Solid State Devices and Materials, Sendai, 1990, pp. 167-170

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MOS Characteristics and Reliability of Thin Gate Dielectrics Grown by Rapid Thermal Processing in O_2 Diluted with NF_3

G. Q. Lo, W. Ting, D. L. Kwong, J. Kuehne* and C. W. Magee**

Microelectronics Research Center,
The University of Texas at Austin,
*Texas Instrument Inc., **Evans East Inc.

High quality ultrathin fluorinated gate oxides by rapid thermal processing in diluted NF_3 and O_2 have been fabricated and characterized. Fluorinated oxides with small amounts of F show less interface state generation under F-N injection, whereas excessive F incorporation deteriorates the interfacial resistance. Increased hole trap density in fluorinated oxides was also observed. In addition to passivating Si dangling bonds, F is speculated to create nonbridging oxygen centers and/or oxygen deficiencies and enhances positive charge trapping during hot-electron injection.

Recently it was found that by incorporating small amounts of F into SiO_2, the MOS device properties could be greatly affected.[1-7] Various techniques have been proposed and studied, including rinsing Si substrates in HF solution prior to oxidation,[1,2] F ion-implantation into poly-Si gate followed by drive-in,[3-6] and furnace oxidation in an O_2 + NF_3 mixture.[7] Proper amounts of fluorine in the oxide was found to suppress hot-electron induced interfacial degradation and enhance radiation hardness, while excessive F incorporation exhibited detrimental effects.[3,4] In order to precisely control oxide thickness (< 10 nm) and F incorporation, rapid thermal processing (RTP) is the most promising candidate since both the NF_3 purging time and oxidation time can be accurately controlled and a low thermal budget is also maintained. As a consequence, RTP is applied in this study to prepare high-quality ultrathin (~10 nm) fluorinated SiO_2 suitable for MOS device applications. The Si substrate temperature and the NF_3 flux were used as switches to turn the surface reaction on or off. Precise and selective F incorporation can be achieved thereby.

The substrates used were (100) oriented P-type Si wafers with a resistivity of 1-2 Ω·cm. The control oxide was grown by RTO at 1050 °C in pure O_2 for 60 s. Two groups of samples were prepared. In the first group, wafers received rapid thermal annealing (RTA) in diluted NF_3 (100 ppm in N_2) prior to gate oxidation with durations from 10 to 40 s at 900 °C followed by an *in-situ* RTO in pure oxygen at 1050 °C for 60 s. In the second group, diluted NF_3 was added to pure O_2 during the 1050 °C, 60 s RTO with NF_3 flowing durations from 10 to 60 s. MOS capacitors were fabricated using standard poly-Si gate technology after gate oxide preparation.

Secondary ion-mass spectrometry (SIMS) was applied to investigate F distribution in the oxide. Fluorine pile-up at the oxide surface was observed with the concentration decreasing toward the Si/SiO_2 interface in the sample received RTA in NF_3 at 900 °C for 20 s before RTO, , as shown in Fig. 1 (a). We believe a significant amount of fluorine is adsorbed on the surface during RTA in NF_3 due to the high temperature and is subsequently incorporated into the oxide during gate oxidation. This process is similar to rinsing wafers in HF before

gate oxidation. On the other hand, fluorine pile-up at both the oxide surface and the Si/SiO_2 interface was observed in the sample grown in O_2/NF_3 with NF_3 purging for 10 s during a 60 s RTO, as shown in Fig. 1 (b). From these profiles, we have demonstrated that significantly different F distributions can be obtained by using different techniques to introduce fluorine. It is also interesting to note that no detectable amount of nitrogen was found in any of the fluorinated samples and, contrary to the work of Nishioka *et al.*,[2] only small amount of ^{47}SiF was detected in all samples.

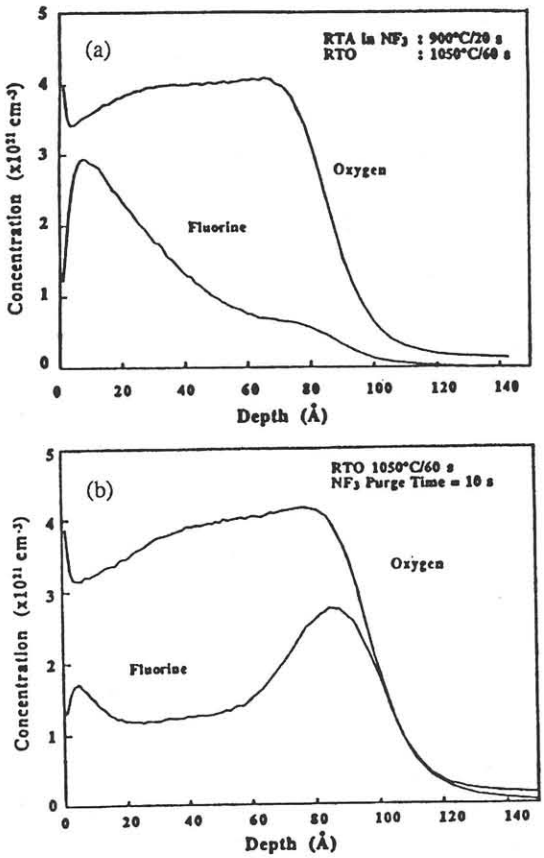
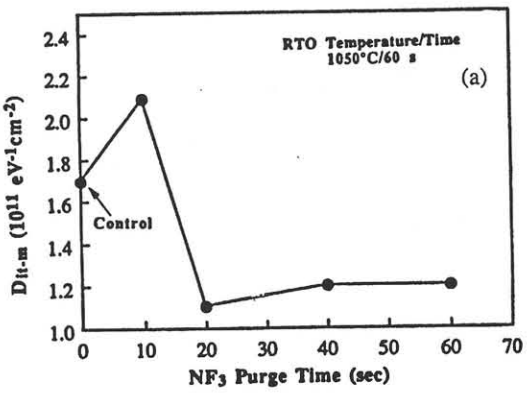


Fig. 1 SIMS depth profiles of O and F obtained from (a) sample rapid thermal annealed in NF_3 at 900°C for 20 s before RTO and (b) sample having NF_3 purging during the first 10 s of RTO. RTO was performed at 1050 °C for 60 s.

The interface state densities (D_{it}) measured by the high-low frequency C-V technique on fresh capacitors are summarized in Fig. 2 (a) and (b) as a function of NF_3 purging time during RTO, and RTA duration in NF_3 prior to RTO, respectively. In Fig. 2 (a), D_{it} decreases as the purge time increases except for the sample which had the shortest, i. e. 10 s of purging. D_{it} in Fig. 2 (b) decreases monotonically with increasing RTA time in NF_3. Nishioka *et al.* suggested that the reduction of D_{it} by NF_3 treatment is due to F tying to the Si-dangling bonds which cannot be terminated by H.[3]

Fig. 3 shows the high- and low-frequency C-V characteristics of MOS capacitors with (a) control oxide, (b) fluorinated oxide prepared with NF_3 purging during RTO, and (c) fluorinated oxide prepared with RTA in NF_3 prior to RTO. Curves obtained from devices before and after F-N electron injection are both presented. In Fig. 3 (b), the quasi-static C-V curves after electron injection from both polarities are less distorted than either Fig. 3 (a) or (c), indicating an enhanced resistance to D_{it} generation. In addition, the shift of high-frequency C-V curve after stressing in Fig. 3 (b) is the least, especially when electrons are injected from the substrate where no shift is observed. The sample which received RTA in NF_3 prior to RTO, on the other hand, exhibited deteriorated resistance to D_{it} generation and increased ΔV_{fb} as compared with the control oxide. Referring to Fig. 1 (a) and (b), the devices shown in Fig. 3 (b) and (c) have very different F distributions, and it is clear that the hot-electron hardness is improved by proper amounts of F at the Si/SiO_2 interface instead of at the SiO_2/gate interface.



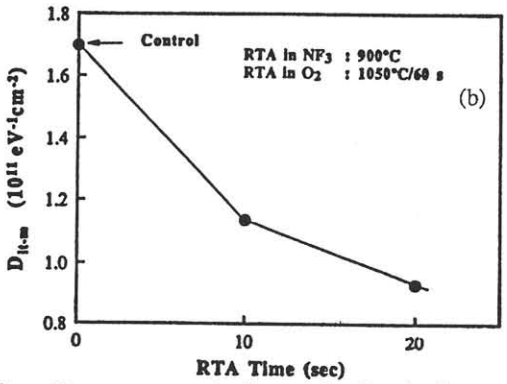
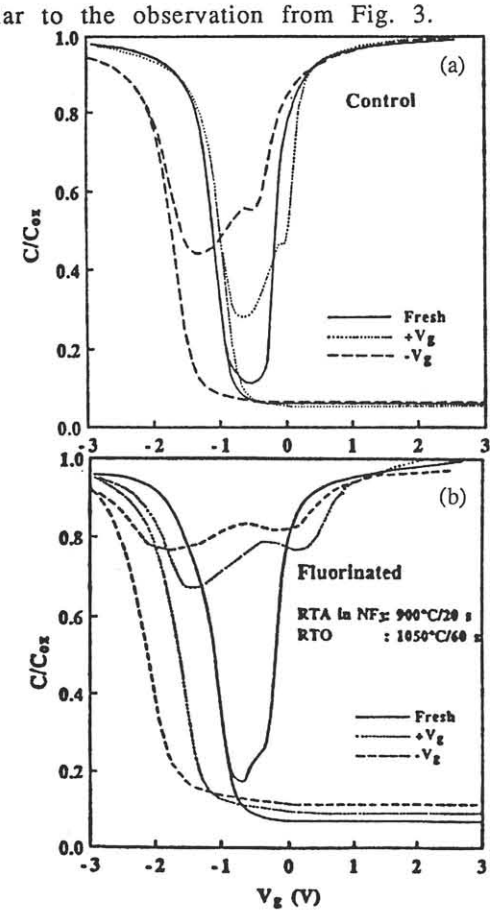


Fig. 2 D_{it} measured from fresh devices as a function of (a) NF_3 purge time during RTO and (b) RTA duration in NF_3 before RTO.

The dependence of hot-electron resistance on NF_3 purge time was also studied and shown in Fig. 4 (a) and (b). All devices were subjected to electron injection to a total fluence of 5 x 10^{-3} C/cm^2. As compared with the control oxide, the sample which received 10 s of NF_3 purge during RTO showed less D_{it} generation while longer purges degraded the hardness. On the other hand, the pre-oxidation RTA in NF_3 for 20 s obviously degraded the hot-electron resistance, similar to the observation from Fig. 3.



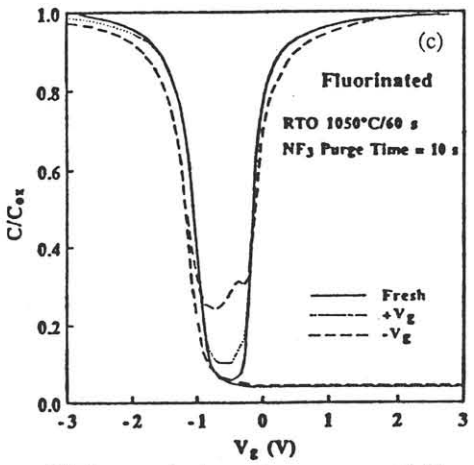


Fig. 3 High- and low-frequency C-V curves measured from MOS capacitors before and after a 300 s constant current stressing. The stress current density was 17 $\mu A/cm^2$. (a) control oxide, (b) fluorinated oxide with NF_3 purging during the first 10 s of RTO, and (c) fluorinated oxide formed by RTA in NF_3 at 900 °C for 20 s followed by RTO.

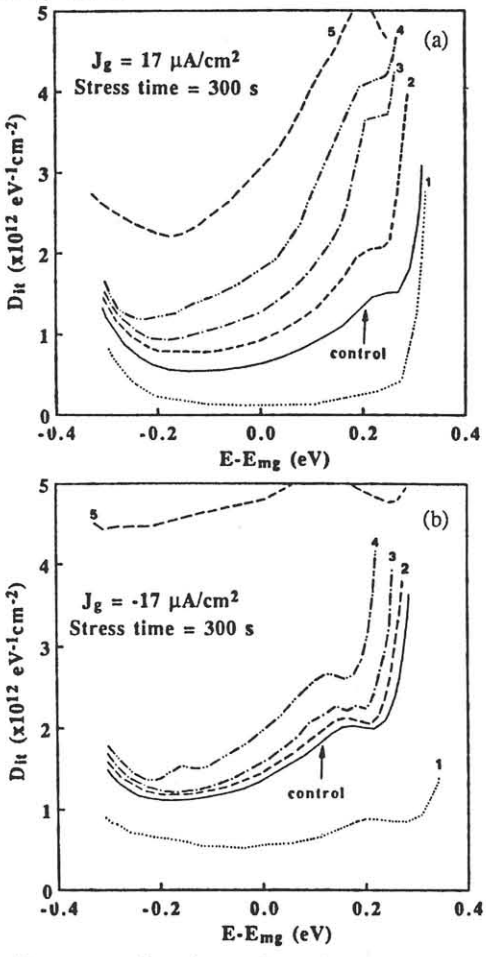


Fig. 4 D_{it} as a function of surface potential after F-N electron injection with NF_3 purge time as a parameter: (a) positive gate bias (b) negative gate bias. Control and fluorinated oxide with RTA in NF_3 at 900°C for 20 s before RTO (labeled

5) are also included. Labels from 1 to 4 represent NF_3 purge time of 10, 20, 40, and 60 s, respectively.

The charge trapping properties of fluorinated oxides under F-N electron injection were also investigated and shown in Fig. 5 in which ΔV_{fb} is plotted against NF_3 purge time during RTO. Negative ΔV_{fb} was observed in all samples under negative gate bias which indicates positive charge trapping. For pure oxide the negative ΔV_{fb} is attributed to donor-type slow interface state generation and/or trapped holes.[8,9] The sample which received 10 s NF_3 purge during RTO showed reduced positive charge trapping compared with control oxide, as indicated by a less negative ΔV_{fb}. Prolonged NF_3 purge, on the other hand, enhances hole trapping. Similar behavior was observed under positive gate bias. The increased hole trap density is speculated to arise from defects such as oxygen deficiency resulted from F incorporation. Similar explanation was proposed for lightly nitrided SiO_2 films.[10] The enhanced positive charge generation in fluorinated oxides due to irradiation has also been reported in which the creation of nonbridging oxygen or E' centers was suggested.[11]

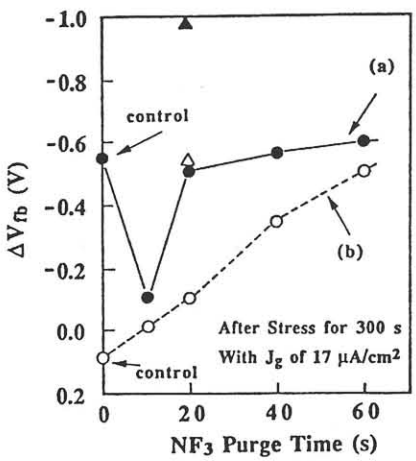


Fig. 5 ΔV_{fb} after F-N electron injection in fluorinated oxide as a function of NF_3 purge time: (a) positive gate bias and (b) negative gate bias. Control oxide and oxide with RTA in NF_3 at 900°C for 20 s before RTO are also included.

In conclusion, MOS characteristics of ultrathin oxides received different rapid thermal treatment in O_2 and NF_3 have been studied. The presence of NF_3 during RTO was found to reduce initial interface density. Process dependence of ΔV_{fb} and ΔD_{it} has been studied and the physical mechanisms have been discussed.

This work was supported by SRC/SEMATECH and Texas Advanced Technology Program.

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