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A Mechanism of Gate Oxide Deterioration Caused by Wafer Charging during Ion Implantation

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Deterioration of oxide films caused by wafer charging during ion implantation was investigated. The effect of ion beam density, the distribution of the deterioration over a wafer and the effect of photoresist coverage are discussed. It is shown that the four charge sources contribute to the deterioration of the oxides: the irradiated ions, the secondary electrons emitted from a gate electrode, the charges accumulated on the photoresist around the gate electrode and the secondary electrons emitted from a wafer holder.

1. INTRODUCTION

Recently, high current implanter has come into use to dope the region such as source/drain of MOSFET for shorter processing time. The resultant charge deposition may cause damage to the silicon dioxide.[1,2] The use of thinner gate oxide and higher beam current will make devices more susceptible to the charge accumulation leading to reductions in yield and long-term reliability. Several factors such as the density of ion beam and photoresist layout affect the degradation of gate oxides.[2,3,4] However, it has not been made clear how those factors relate to charging damage to the gate oxides in microscopic device structures. In this paper, we show quantitatively that the gate oxide deteriorates with the increase of ion beam density. Effects of secondary electrons emitted from both a wafer holder and a gate electrode are discussed. Furthermore, it is shown that a photoresist layer promotes the deterioration of oxide films.

2. EXPERIMENTAL PROCEDURE

Figure 1 shows the schematic diagram of the ion implanter which was used. Wafers with MOS capacitors are mounted on the disc which is made of aluminum metal. During implantation, the disc rotates at the speed of 300 revolution per minute and moves toward the radial direction. Ion beam distributions are measured by a beam profile monitor which consists of arrays of small Faraday cups. Positive arsenic ions with the kinetic energy of 35 KeV were implanted to the wafers. The total dose of implanted

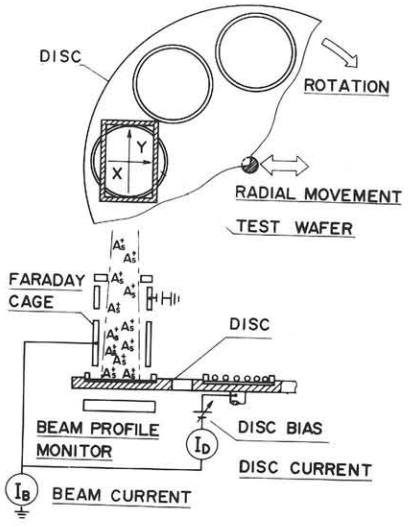


Fig.1 Schematic diagram of ion implanter.

ion was controlled to be $3x10^{15}$ ions/cm^2 in all the experiments. Test capacitor devices consist of polysilicon, thin silicon dioxide(25nm), and substrate silicon as shown in Fig.2. The area of the polysilicon electrode and the oxide film is $4.2x10^{-3}cm^2$ and $3x10^{-3}cm^2$, respectively. The devices were fabricated on n-type 150mm diameter (100) silicon substrates. Interface state(at 0.25 eV above the midgap of silicon) generated at Si/SiO2 was used as an indicator of oxide degradation by measuring quasi-static capacitance voltage(C-V) curves.

3. EXPERIMENTAL RESULTS AND DISCUSSION

3.1 Effects of Ion Beam Density

Firstly, we examine the effect of ion beam density which can be regarded as the primary factor causing oxide deterioration in implantation process. Figure 3 shows the dependence of interface state density(ΔDit) on the peak current density of irradiated ion beam. The peak current density was varied from 1.4 mA/cm^2(Beam A) to 0.12mA/cm^2(Beam E). We clearly observed increase of interface states with the increase of ion beam density as shown in Fig.3. The polysilicon(250nm) electrode covering the gate oxide is thick enough to prevent As^+ from penetrating into the gate oxide. Therefore, we do not need to take account of the possibility of interface state generation due to the penetration of ions. The interface states are considered to be generated by charges passed through the oxide during implantation. Since the total dose of ion for each implantation was controlled to be $3x10^{15}$ ions/cm^2, the number of positive charges passed through the oxides must have been the same in the five different ion beams. Therefore, the dependence on beam current indicates that the electric field induced by beam current in the oxide accelerates the generation of interface states even if the total dose are the same.

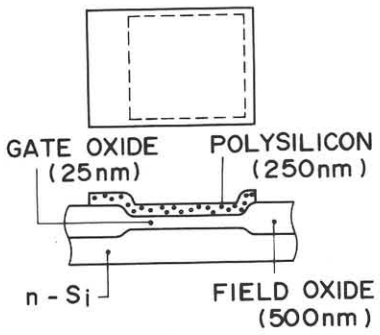


Fig.2 Cross sectional view of MOS capacitor.

3.2 Distribution of Damage over a Wafer

To improve production yield, the distribution of damage over a wafer must be clarified. In this section, we show that non-uniform deterioration is brought about by the secondary electrons emitted from the aluminum metal around test wafers.

Figure 4 shows the interface state density of MOS capacitors which are located at five different positions on a wafer. The interface state is substantially generated for the MOS capacitors situated at around the wafer center while the generation is small at the wafer edge. Basically, the gate

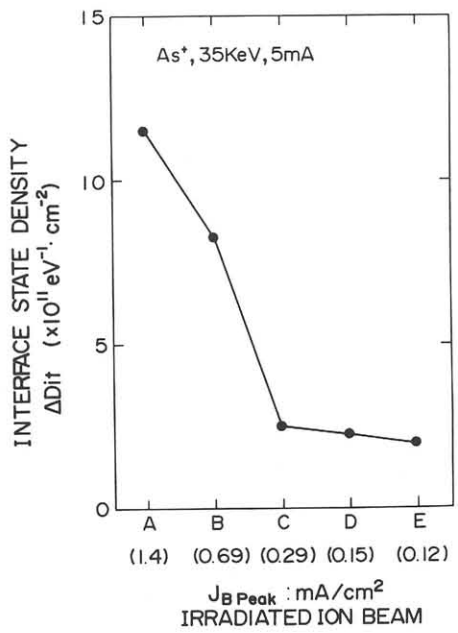


Fig.3 The dependence of interface state density on the peak beam current density.

oxide deteriorates with the passage of the charges accumulated on the gate electrode. Therefore, if only the positive charges transported by ion beam is the cause of current stress to the oxides, the MOS capacitors should degrade uniformly over the wafer because the ions are uniformly deposited. However, the interface state density at the wafer edge is far lower than that near to the wafer center. This experimental result suggests that the capacitors at the wafer edge are supplied with negative charges which compensate the positive ion charges. It is most likely that the aluminum metal around the wafer is the source of electrons because ion beam irradiates the surface of aluminum disc around wafers as well as the wafers themselves. Figure 5 shows the currents(I_{SE}) due to secondary electrons from the aluminum and silicon targets at various voltages of the disc bias. The value of I_{SE} at the saturation voltage indicates that aluminum can generates 6 times electrons as many as irradiated As^+ ions. The number of electrons is enough to neutralize positive charges of propagating ions to the wafers when the circumferential part of the wafer is irradiated. The role of the secondary electrons emitted from the silicon surface of gate electrodes will be described in the section 4.

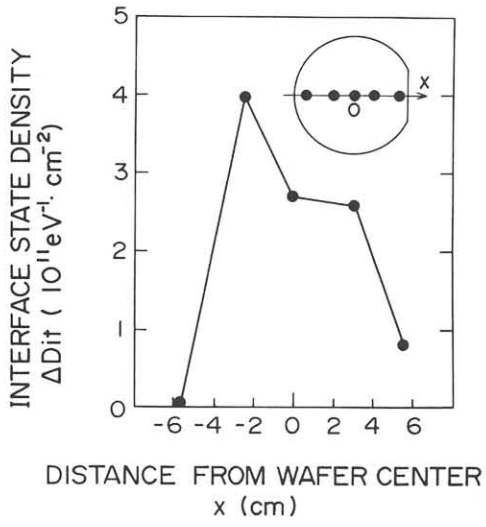


Fig.4 The dependence of interface state density on the position over a wafer.

3.3 Effect of Photoresist Coverage

As an usual structure of wafers in implantation process, some portions of the wafer surface are covered with photoresist layer to prevent ion deposition to undesirable regions. In this section, we show that a layout of photoresist can accelerate the deterioration of gate oxides.

Figure 6 shows the effect of photoresist coverage. The interface state density caused by implantation was compared using the capacitors A1 and A2 on different wafers. The photoresist layer(1um) surrounds the gate electrode of capacitor A1, while photoresist was not coated around capacitor A2. As shown in Fig.6, the interface state

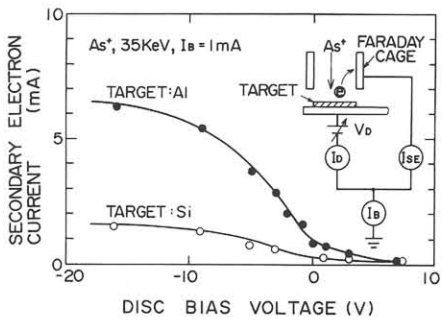


Fig.5 The secondary electron current from aluminum and silicon versus the bias voltage applied to the disc.

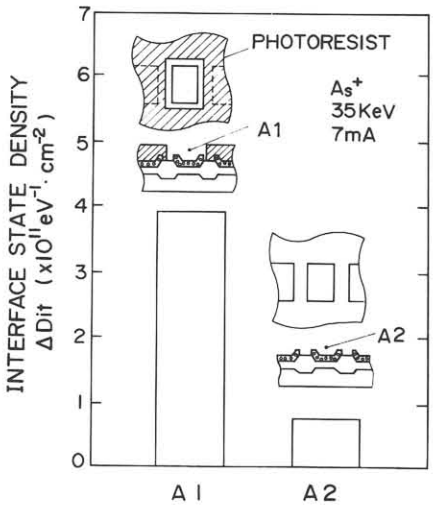


Fig.6 The dependence of interface state density on the photoresist coverage. The photoresist layer surrounds the gate electrode of capacitor-A1 and is not coated on the capacitor-A2 wafer.

density of capacitor A1 is five times as high as that of capacitor A2. The number of charges which passed through the gate oxide of capacitor A1 is more than that of capacitor A2. This shows that the deterioration of gate oxide strongly depends on how photoresist covers the gate electrode of the capacitor.

4. MECHANISM OF DETERIORATION OF GATE OXIDE

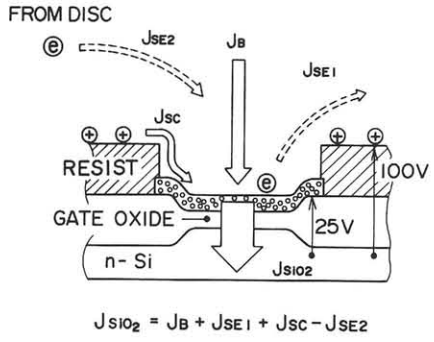
The deterioration mechanism of MOS capacitor surrounded by photoresist layer can be explained by four components (J_B, J_{SE1}, J_{SC}, J_{SE2}) of gate current(J_{SiO2}) shown in Fig.7.

Firstly, the beam current density(J_B) is a major factor as mentioned in section 3.1.

Secondly, the current due to secondary electron from the gate electrode(J_{SE1}) increases the gate current. This is explained as follows. The potential of the gate electrode stays below 27 V because it cannot be over the breakdown voltage of the oxide, while the potential of the photoresist surface can become about 100 V with respect to the substrate silicon as reported.[5] The potential difference drives the secondary electrons to the surface of the photoresist layer leaving additional positive charges on the gate electrode.

Thirdly, the current due to positive charges of ions accumulated around the gate electrode (J_{SC}) is involved. The difference of 5 times of ΔDit between capacitor A1 and A2 in Fig.6 can not be explained only by the secondary electrons from the gate electrode because the electrons can increases the gate current by 1.5 times the beam current at most as expected from Fig.5. Therefore, considering the potential of the gate electrode to be the lowest, it is assumed that the positive charges on the photoresist surface are conducted along the photoresist surface toward the gate electrode.

Finally, the current due to secondary electrons from a wafer holder (J_{SE2}) decreases the gate current especially for the capacitors at the wafer edge.



$J_{SiO_2} = J_B + J_{SE1} + J_{SC} - J_{SE2}$

Fig.7 The sources of charges and its path toward the gate oxide during ion implantation.

5. SUMMARY

We have investigated how the gate oxide deteriorates during ion implantation. The following four types of charges were found to affect charging damage to gate oxides during ion implantation: ion beam irradiated into the gate electrode, secondary electrons emitted from the gate electrode, positive charges accumulated around the gate electrode, secondary electrons emitted from a wafer holder.

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