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Novel Selective Platinum Deposition on VLSI Contact Hole

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The non–contamination selective electroless deposition of platinum was innovated. The excellent selectivity of Pt deposition into Si contact holes of 2 μm is shown. The compositions of the deposited Pt film on (100) silicon substrate was identified by the EDAX spectrum. Only platinum and silicon are detected which indicated that deposited Pt film is clean and pure. The resistivity of the deposited platinum film is 10.8 Ω–cm . We realized a low contact resistance of 76 Ω–μm^2 on p^+ diffusion layer .

1. Introduction

The multilevel interconnect and contact hole filling are two main challenging issues in submicron VLSI technology. In conventional evaporation or magnetron sputtering metalization, the step–coverage of the film over via hole is poor and becomes worse as the dimension shrunk down. The step–coverage problem can be solved if the vias are filled by plug of metal, which also promotes the planarization of multilevel metalization. In the recent years, the selective electroless metal deposition (SEMD) technique has been developed to solve the problems metioned above. It is a process of low cost and high throughput, and much simpler than CVD Tungsten. In this paper, a novel selective electroless Pt deposition was investigated. Using this method, we realized (1) pure Pt deposition on Si, (2) excellent selectivity between Si and SiO_2, (3) PtSi formed after annealing, and (4) low contact resistance of 76 Ω–μm^2 on P^+ Si diffusion layer. The P^+/N shallow junction of 0.21 μm was fabricated to examine the quality of Pt silicide, the ideality factor of forward bias is 1.096 and the leakage current of reverse bias of –5 volts is 6.3 $\mu A/cm^2$.

2. Process and Results

Phosphorous doped n type (100) Si wafers with resistivity of 3.5 Ω–cm were empolyed in this work. The recipe of chemical solution of electroless Pt deposition is shown in Table 1. In Table 2, the process sequence is presented. After RCA cleaning and diluted HF dipping, the samples were immersed immediately into the sensitization solution for 1 minute. The stannous ions adsorbed on the surface of

samples, since the HF in sensitization etched the SiO_2 surface, therfore, the stannous ions adsorbed on the Si surface only. Then, immersion of 1 minute pre–deposition was followed by 5 minutes D.I. water rinse. At last, Pt SEMD was performed at 80–100°C. The concept of Pt SEMD is to reduce Pt ions through the interaction between Pt ions and the reducing agent Sn^{2+} at the Si surface. The oxidation–reduction reaction is described as below:

$$Pt^{4+} + 2\,Sn^{2+} \longrightarrow Pt_{(s)} + 2\,Sn^{4+}$$

Thus the Pt particles deposited on Si surface but not on SiO_2 surface. Fig.1 shows the EDAX diagram of the as–deposited Pt film. Only Pt and Si were dectected, so it was pure Pt deposition. The top view and cross section of SEM of as–desposited Pt films were shown in Fig.2 (a) and (b), respectively. The deposition of Pt particles on Si surface, not on SiO_2 surface, is shown in Fig.3 (a). And the grain sizes of Pt particles range from 0.2 to 0.4 μm. Fig.3 (b) shows the excellent selectivity of Pt deposition into contact holes. In order to form Pt silicide,the Pt SEMD was annealed at 800°C for 30 minutes in vacuum (10^{-5} Torr). The result is shown in Fig.4. Most of the deposited Pt was converted into PtSi. Fig.5 is the cross–section of STEM of PtSi silicide. The contact resistance between PtSi/Si was measured by 6–terminals Kelvin technique. The relation between resistance and contact area is shown in Fig.6, the contact resistance is 76 Ω–μm^2. Shallow juction P^+/N diodes were fabricated to examine the device performance. Fig.7 (a),(b) were measured I–V under forward and reverse bias, respectively. From Fig.7 , the ideality factor is 1.096 and the leakage current density is 6.3 $\mu A/cm^2$ at reverse bias of –5 volts.

3. Conclusions

The selective electroless Pt deposition on Si was successfully achieved. The as–deposited Pt film was pure, and Pt silicide was formed after annealing. A low contact resistance of 76 Ω–μm^2 was suitable for VLSI devices. The P^+/N shallow junction of 0.21 μm was fabricated to examine the quality of Pt silicide, the ideality factor of forward bias is 1.096 and the leakage current of reverse bias of –5 volts is 6.3 $\mu A/cm^2$.

4. Acknowledgement

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5. References

(1) C.S. Wei et al., IEDM Tech. Dig., P.449 ,1988

(2) P.L. Pai et al., Proc. 5th Int IEEE V–MIC, p.331, 1988

(3) P.L. Pai et al., IEEE Electron Device Letters, vol.EDL–10, no. 6, p.423. 1989

(4) M. Wittmer et al., J. Appl. Phys. 54,

p.5081, 1983.

(5) S.P. Murarka et al., J. Vac. Sci..Technol.B5, p.1674, 1987.

(6) S.S. Cohen et al., AP, INC., New York, 1986.

Table.1 The recipe of the solutions of Pt SEMD.

sensitzation	$SnCl_2 \cdot 2H_2O$	5 g/l
	HF	1 %
	Room Temperature	
	1 min	
Pre-deposition	$H_2PtCl_6 \cdot 6H_2O$ (10%)	5 ml/l
	HF	1 %
	Room Temperature	
	1 min	
Electroless Pt deposition	$H_2PtCl_6 \cdot 6H_2O$ (10%)	20 ml/l
	NH_4Cl	40 g/l
	NH_4OH	PH 9-10
	NH_2NH_2	0.1 g/l
	boiling	

Table.2 The process sequence of Pt SEMD.

Sequence	Process Step
1.	(100) Si substrate cleaning
2.	Thermal oxidation (0.5 um)
3.	Contact hole openning
4.	Sensitization
5.	Rinse in D.I. water 5 mins
6.	Pre-deposition
7.	Rinse in D.I. water 5 mins
8.	Electroless deposition

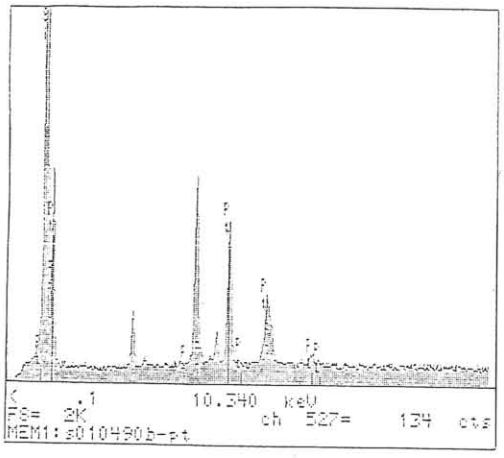


Fig. 1 The EDAX spectrum of the Pt SEMD , only Pt and Si Peaks were detected.

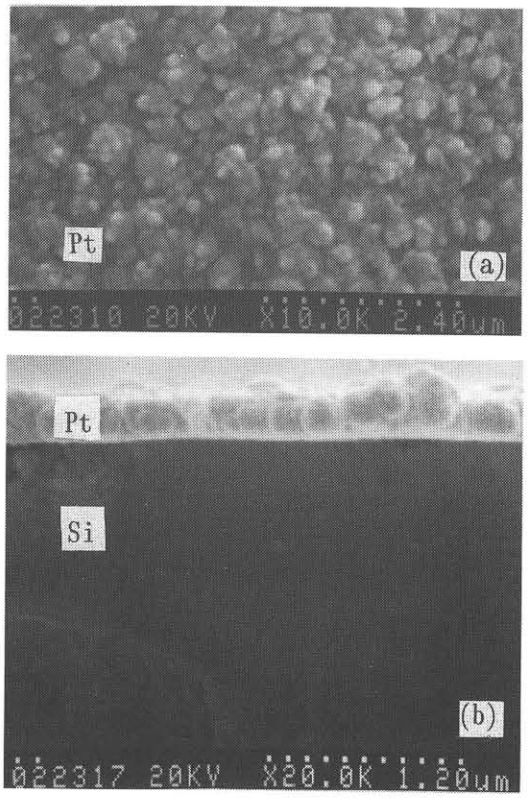


Fig.2 The SEM pictures of the as-deposited Pt films. (a) The top view and (b) the cross section , respectively.

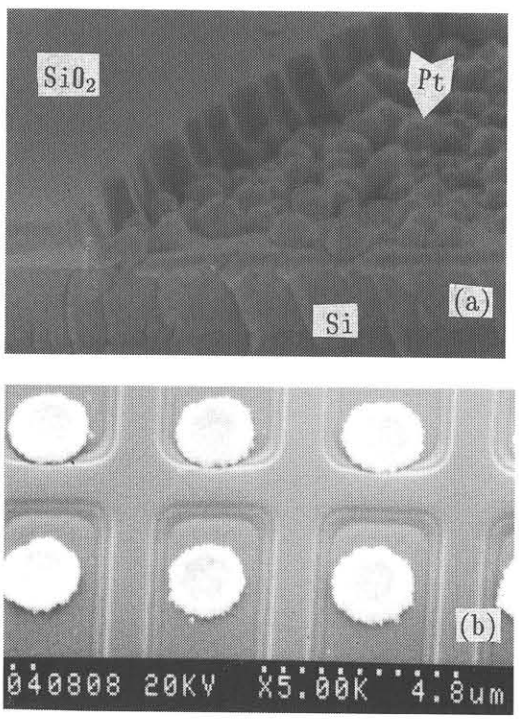


Fig.3 The SEM pictures of Pt SEMD. (a) Pt particles deposited on Si surface only. (b) the Pt filled into the contact hole of 2 μm.

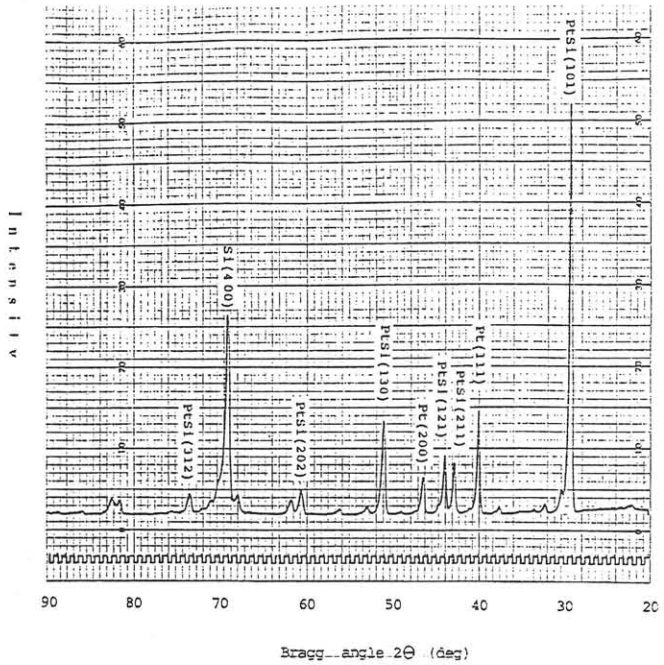


Fig. 4 The X–ray diffraction spectra of Pt SEMD which was annealed in vacuum at 800 °C for 30 mins.

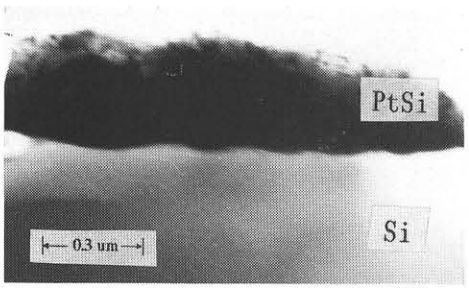


Fig.5 The STEM picture of the cross section of PtSi formed at 800°C annealing.

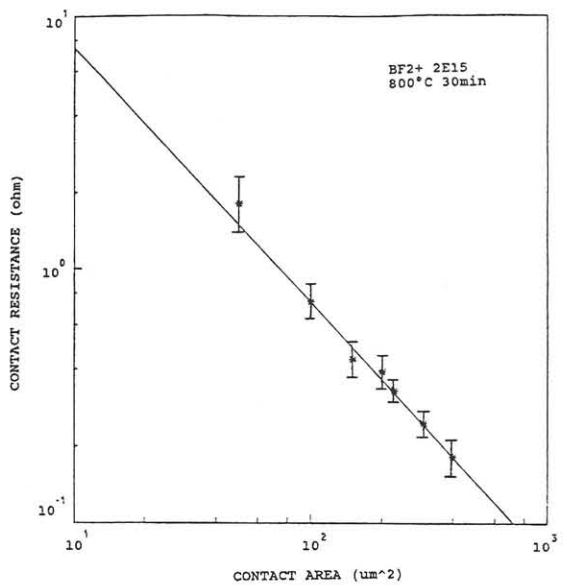
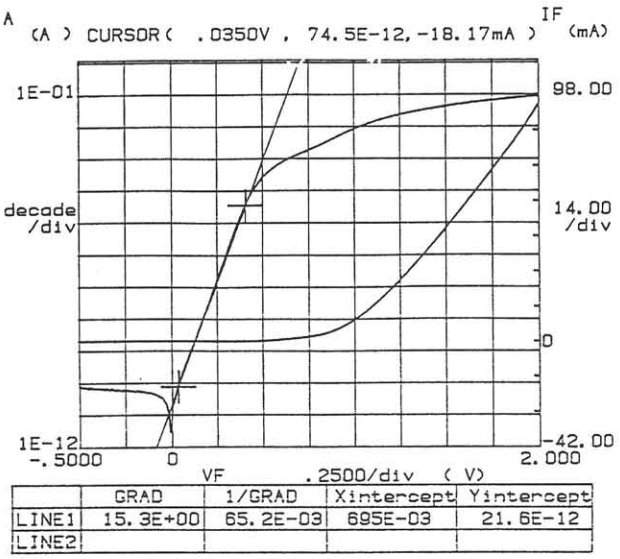
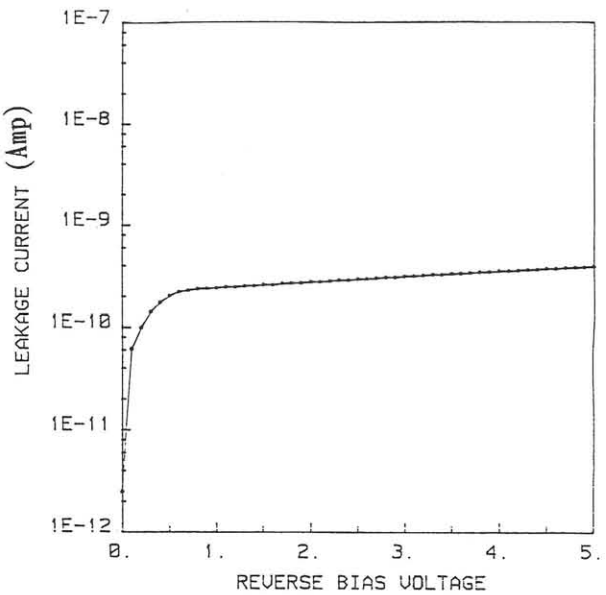


Fig.6 The measured contact resistance vs. the contact area of the PtSi/P⁺ – Si. The contact resistance is 76 Ω–μm².



(a) forward bias



(b) reverse bias

Fig.7 The I–V characteristics of Pt SEMD on the shallow P⁺/N junction after annealing at 800°C for 15 mins. Area is 6400 μm².