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Performance of Extrinsic and Intrinsic MOSFETs in Deep Submicron VLSI

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The performance of the MOSFETs with advanced hot carrier resistant source/drain structures in deep submicron range was investigated. As device performance indicators the current drive capability and the transconductance of the intrinsic MOSFETs were used. They were determined by using a new methode providing autocorrection for the operating point dependent series source/drain resistances. Typical LDD nMOSFETs in the 16M technology were investigated. The maximum possible intrinsic transconductance for different oxide layer thicknesses and the inversion layer thickness were experimentally determined. Gate oxides with thicknesses down to 3-5nm can be used to increase the intrinsic device performance without significant limitation due to the finite inversion layer capacitance. The results on the performance of the extrinsic and intrinsic MOSFETs, especially in the deep submicron range, suggest the need for a come-back of the abrupt source/drain profiles without LDD extensions and for a corresponding reduction of the supply voltage to reduce hot carrier effects.

1. INTRODUCTION

The parasitic effects due to the source/drain series resistances on MOSFETs characteristics have long been known [1-4], but they were negligible for conventional MOSFETs with deep abrupt source/drain junction profiles and larger channel lengths. In this case, the series resistances are independent of the operating voltages.

In advanced VLSI, however, the problems due to the source/drain series resistances become increasingly severe and complicated, especially when the feature sizes are progressively shrunk into the deep submicrometer range. Shallow junctions with LDD extensions or with other graded junction profiles are used to reduce hot carrier effects. These hot carrier resistant source/drain structures exhibit obviously high parasitic series resistances which, however, do not explicitely show up in sophisticated 2D-simulations. Therefore, an alternative interpretation of the simulated device performance in terms of the parasitic series source/drain series resistances is not possible. Thus, any improvement of the hot carrier immunity by using LDD structures is viewed as a benefit. Up to now, little attention has been paid to the performance limitation associated with the increased series resistances. These resistances can only be determined from the simulated I-V data by using additional extraction procedures [5].

It has been shown that some resistance components such as the spreading- and the accumulation layer resistances are strongly dependent on the gate voltage [6]. Due to the graded junction profiles, the effective channel length and the series resistances are interdependent [7]. Thus, the electrically effective channel length itself is strongly gate voltage dependent, too. The impact of these gate voltage dependences and the related effects on device performance has not been reported, up to now.

The main purpose of this work was to clarify the significance of the gate voltage dependent parasitic series resistances for the device performance and to determine their importance relative to the other limitations in the deep submicrometer range. To this end, the current drive capability and the transconductance of the intrinsic devices were measured and used as device performance indicators. To determine them, a new auto-correction procedure for R_s and R_d was developed. The bias dependent parameters R_s, R_d and L_{eff} were determined electrically using dual linear least-square fit methods similar to [7]. With the auto-correction for Rs and Rd, the performance of the intrinsic device was determined experimentally in the entire range of the MOSFET operating voltages. Results are given for typical LDD nMOSFETs fabricated in a 16M process. The LDD junction profiles were optimized with respect to the hot carrier immunity at 5V operation.

2. THE SOURCE/DRAIN SERIES RESISTANCE

Fig.1 shows the measured parasitic source resistance R_s' of nMOSFETs with LDD extensions vs. gate voltage. The strong dependence on the gate voltage is evident. The magnitude of R_s' is in the kΩ*μm range. This is much higher then the tolerable parasitic source resistance of a few hundert Ω*μm (228 Ω*μm) as given in [8] for the 1/4 micrometer channel level.

Fig.2 shows the difference between the drawn channel length L_g and the electrically effective channel length L_{eff}, $dL_e = L_g - L_{eff}$ as a function of the gate voltage. The gate voltage dependence of the effective channel length is significant. The change of the effective channel length is about .1 μm if V_{gs} changes from 3V to 5V.

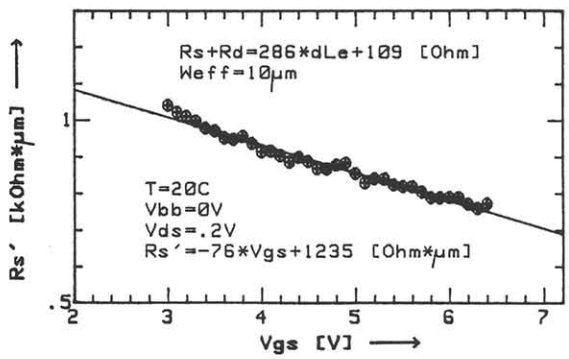


Figure 1. Gate voltage dependent source series resistance of nMOSFETs with LDD extensions R_s' normalized to 1μm channel length.

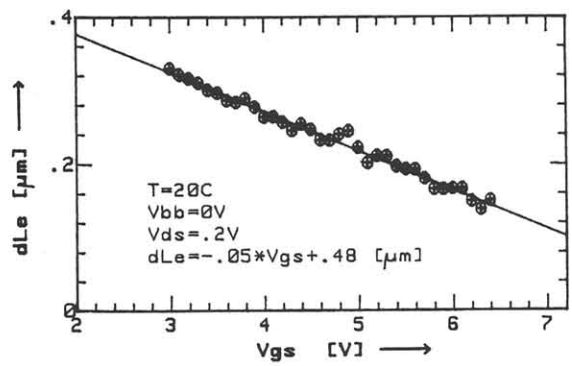


Figure 2. Gate voltage dependent effective channel length defined by $dL_e = L_g - L_{eff}$ for nMOSFETS with LDD extensions.

Figures 1 and 2 show clearly that the series resistance and the effective channel length are interdependent. Increasing the gate voltage, R_s' is decreasing and the effective channel length is increasing. The interdependence between $R_s + R_d$ and L_{eff} is given in Fig.1.

The voltage drops on the R_s and R_d cause parasitic biasing of the internal source-, drain- and substrate terminals. The corresponding reductions of the intrinsic gate-, drain- and the substrate voltages are functions of the drain current. But the drain current itself is determined by the internal biases. Thus an electrostatic feedback exists between the internal biases and the drain current as can be seen from Eq.(1):

$$I_d = W_{eff}/L_{eff} * \mu_n * C_{ox} * (V_{gs}' - V_T') \qquad (1)$$

where the internal gate to source voltage $V_{gs}' = V_{gs} - I_d * R_s$. The threshold voltage V_T' corresponds to the internal voltages $V_{ds}' = V_{ds} - I_d * (R_s + R_d)$ and $V_{bs}' = V_{bs} - I_d * R_s$. The internal gate drive $V_{gs}' - V_T$'now is a function of the drain current. Because of the threshold sensitivity to the internal drain- and substrate voltages, V_T' becomes larger. The higher the drain current the smaller the intrinsic gate drive becomes. Therefore, the feedback is negative. The negative feedback allows to provide an auto-correction for R_s and R_d. The internal gate drive can be kept constant by using iterative current measurements, hence, the voltage drops on Rs and Rd are known. The voltage drops on R_s and R_d can reach high values, especially for MOSFETs in the deep submicron range. They were, up to now, underestimated [9].

3. EXTRINSIC AND INTRINSIC PERFORMANCE

3.1 CURRENT DRIVE CAPABILITY

Fig.3 shows the drain current I_{sq} for nMOSFETs with two different channel lengths normalized to unit channel width and channel lengths (square nMOSFET) as a function of the gate voltage V_{gs}. The drain current curve with $L_{eff} = 0.3\mu$m crosses the curve with $L_{eff} = 0.7\mu$m at about $V_{gs} = 3.5$V. Above this gate voltage, the current of the square nMOSFET with the shorter channel length is lower then that for the longer channel length. This is a consequence of the negative feedback: the reduction of the internal gate drive is higher for the nMOSFET with the shorter channel length due to the parasitic biases

A short-channel MOSFET model including the effect of the

series resistances on the internal gate drive was used to calculate the gate voltages V_{gs} at which the current curves are crossing each other for two different channel lengths. Fig 4 shows the cross-point gate voltage vs. source series resistance R_s' and the measured V_{gs} value for $R_s' = 1k\Omega^*\mu m$.

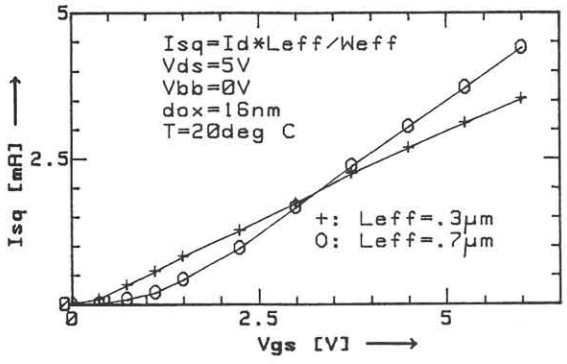


Figure 3. Drain current of square nMOSFETs I_{sq} for two different channel lengths as a function of the gate voltage V_{gs}.

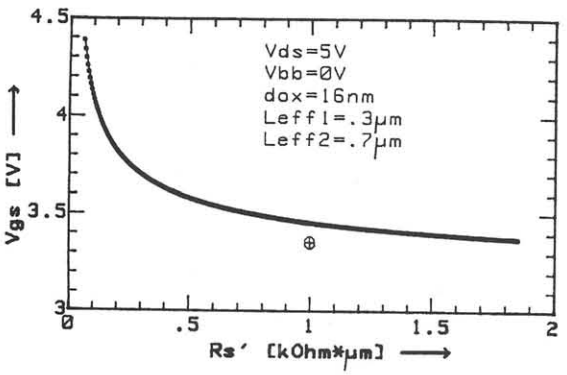


Figure 4. The cross-point gate voltage vs. source series resistance R_s' calculated for drain currents of square nMOSFETs with two different channel lengths.

Fig.5 shows the channel length dependence of the extrinsic and intrinsic drain currents in comparison to the first order 1/L law curve. The difference between the intrinsic-and the extrinsic drain currents is significant. This indicates the need for reduced series resistances, especially in the submicrometer range.
The relative importance of R_s and R_d, compared to all other effects as performance limitation factors, can also be estimated from Fig.5. The difference between the intrinsic drain current and the ideal 1/L dependent drain current can be assigned to other limitation factors as to the saturation of the drift velocity, the mobility degradation and the finite inversion layer thickness.

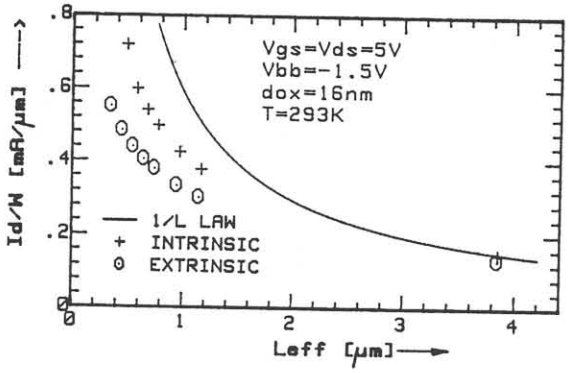
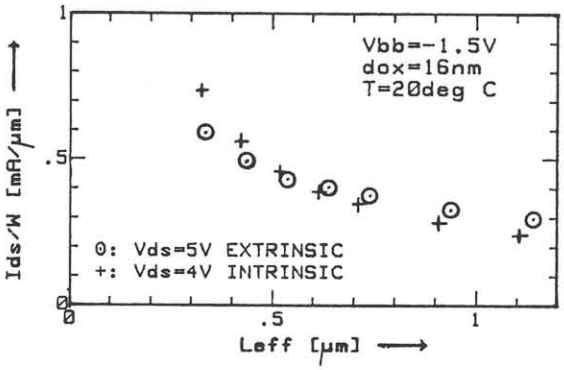


Figure 5. Channel length dependent drain current of the extrinsic, intrinsic and the ideal nMOSFETs determined by auto-correction for R_s and R_d.



Fifure 6. Comparison of the drain currents of the extrinsic nMOSFETs with 5V and the intrinsic nMOSFETs with 4V operation voltages.

The auto-correction for R_s and R_d was used for a lower operating voltage of 4V, too. Fig.6 compares the measured extrinsic drain current at 5V and the measured intrinsic drain current at 4V operation. The nMOSFETs with their high R_s and R_d at 5V exhibit already smaller currents for effective channel lengths below about 0.6μm than the intrinsic nMOSFETs at 4V.

3.2 TRANSCONDUCTANCE

The intrinsic transconductance g_{mi} was extracted from the measured extrinsic transconductance according to (2):

$$g_{mi} = g_{me} / (1 - R_s * g_{me} - Rsd * g_d - Rs * g_b) \qquad (2)$$

where g_{me},g_d and g_b are, by definition, the measured transconductance, drain conductance and substrate

conductance, respectively and $R_{sd}=R_s+R_d$. Gate voltages corresponding to the maximum transconductance were choiced. Values for R_s and R_d at these gate voltages were used. Fig.7 shows g_{mi} as a function of the effective channel length for different oxide thicknesses. An apparent carrier transport velocity, defined as $g_{mi}/(W*C_{ox})$ is also shown. This velocity is found to be largely independent of the oxide thickness. By extrapolating the effective channel length to zero, the maximum intrinsic device transconductance $g_{mi}(0)$ for different oxide thicknesses was determined.

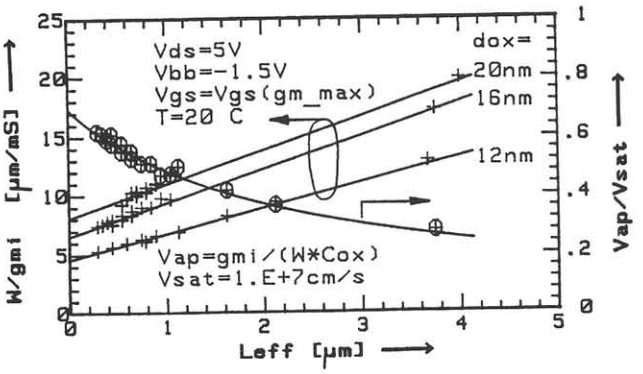


Figure 7. The intrinsic transconductance of nMOSFETs vs. effective channel length for different oxide thicknesses.

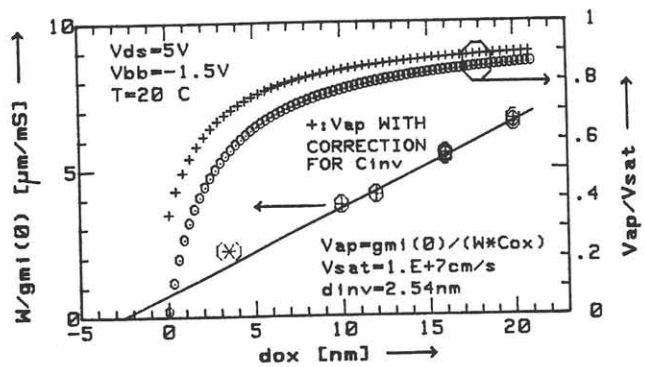


Figure 8. Maximum possible intrinsic transconductance of nMOSFETs determined by extrapolating to zero channel length vs oxide thickness. The apparent carrier velocities V_{ap} with and without correction for C_{inv} are shown, too.

As shown in Fig.8, the inverse intrinsic transconductance $W/g_{mi}(0)$ depends linearly on the oxide thickness (the value for $d_{ox}=3.5$nm is taken from [11]). The intersection of $W/g_{mi}(0)$ with the d_{ox} axis can be assigned to the inversion layer thickness d_{inv}. This allows to determine the inversion layer capacitance C_{inv}. The influence of the finite inversion layer thickness on the apparent carrier velocity can be estimated by correcting for C_{inv} as shown in Fig.8.

About 90% of the saturation velocity is reached for higher d_{ox} values. As expected, V_{ap} decreases strongly for lower d_{ox} values which are comparable to the inversion layer thickness.

4. CONCLUSIONS

The new auto-correction procedures can be used to determine the performance of the intrinsic devices. The presented results indicate that in the deep submicrometer range, the high source/drain series resistances of the LDD extensions strongly decrease the current drive capability and the transconductance of the MOSFETs. This effect was considered to be of little importance, up to now. The methods developed in this work can be used to determine the trade-off between the advantages of the LDD structures with regard to hot carrier immunity and their disadvantages with respect to the drive capability and the transconductance. Oxide thicknesses down to about 3-5nm can be used without significant reduction of the apparent carrier velocity due to the finite inversion layer thickness. The results suggest the need for a drastic reduction of the parasitic resistances by abrupt junction profiles to increase the device performance and for a proper reduction of the supply voltage to reduce hot carrier effects in the near future.

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