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Nanometer Structure of Gate Electrode/Gate Insulator Interface and Anomalous Voltage Deviation of Tunneling Current in Submicron MOS Devices

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Gate polycrystalline silicon/gate insulator interface characteristics is shown to be correlated to Fowler-Nordheim tunneling current flowing through a gate insulator film. When the tunneling area of the current is less than 1 μm^2, there appears an anomalous voltage deviation of the tunneling current. It is also determined that low-temperature processing, a low-phosphorous density for the gate polycrystalline silicon, and a two-layer gate insulator film consisting of Si_3N_4/SiO_2 are effective for reducing the deviation.

Introduction

Gate electrode polycrystalline silicon (poly-Si)/gate insulator interface structures are becoming more important in nonvolatile memories and thin film transistors[1] due to the greater integration of devices. In addition, it has been suggested[2] that undulation at the interface causes the degradation of channel carrier mobility as MOS transistors are further scaled down. However, research on the gate insulator in MOS devices has concentrated on the gate insulator/substrate interface[3-9]. Therefore, the gate electrode/gate insulator interface characteristics[10-13] have not been clarified. In this study, a 1-2 nm high undulation inhomogeneous over the gate poly-Si/gate insulator interface is directly observed. Moreover, it is clarified for the first time that the undulation causes device performance deviation in submicron MOS devices. This deviation has occurred in the form of anomalous voltage deviation of Fowler-Nordheim (F-N) tunneling current, which plays an important role in the write/erase performance of nonvolatile memories.

Experimental

Poly-Si gate capacitors were fabricated in order to observe the gate poly-Si/gate insulator interface structure. The fabrication process was as follows. After Si wafers were oxidized to 11 nm in thickness, a poly-Si film 200 nm in thickness was deposited on them by Low Pressure Chemical Vapor Deposition (LPCVD). Then, P ions ($2x10^{15}$, $1x10^{16}$, $3x10^{16}$ cm^{-2}) were implanted into the poly-Si film. Next, the samples were annealed at high temperature (950, 1050, 1150 °C) for 60 min. Some samples had a two-layer gate insulator film consisting of Si_3N_4/SiO_2. The Si_3N_4 film was deposited by LPCVD to 2.5 nm or 4.8 nm in thickness. In these samples, the interface structure was studied by the direct observation of the exposed insulator surface by high resolution Scanning Electron Microscopy (SEM) after the gate poly-Si film was stripped off the MOS structure by soaking the samples in a hydrazine solution.

Poly-Si gate MOS transistors were made that have a 0.2 μm^2 tunneling area on the source that is overlapped by a gate electrode of phosphorous (P)-doped poly-Si film as shown in

Fig.1. This tunneling area varied with the channel width, while its length along the channel was fixed at 0.2 μm. The Fowler-Nordheim tunneling current between the gate electrode and the source, flowing through the tunneling area, was measured. Then the drain was electrically floated, the substrate and gate electrode were grounded, and positive bias was applied at the source.

Results and Discussion

The current-voltage characteristics with positive voltage on the source have about a 1.5 volt deviation independent of the current density when the tunneling area is 0.2 μm^2 (Fig.1). This deviation occurred due to the scaling down of the devices (Fig.2). Therefore, this phenomenon will become more important as devices are further scaled down. The important thing to note is that the minimum voltage of the deviation is independent of the tunneling area, although the maximum voltage increases as the tunneling area decreases. This indicates that the anomalous voltage deviation is caused by defects in the gate insulator film. In other words, this deviation is explained by assuming that the tunneling current flowing through defects dominates the total current and that a smaller current flows when the tunneling area includes fewer defects. Therefore, this voltage deviation occurs when the sample size is smaller than the area in which the average number of defects is approximately one, because in such a device size the number of defects included is different between measured samples. However, when the tunneling area is much larger than 1 μm^2, the voltage deviation between samples measured is small and independent of tunneling areas. This is thought to be so because the number of defects included in the tunneling area is nearly the same. The above results show that the density of the defects which determines the F-N tunneling current is about 1 μm^{-2}. Therefore, a

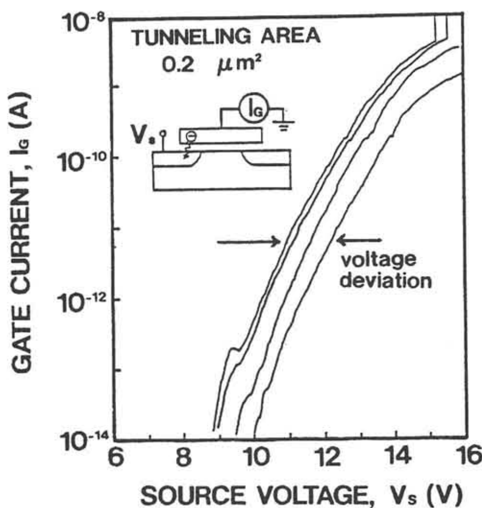


Fig.1 GATE CURRENT versus SOURCE VOLTAGE measured with substrate grounded and drain open

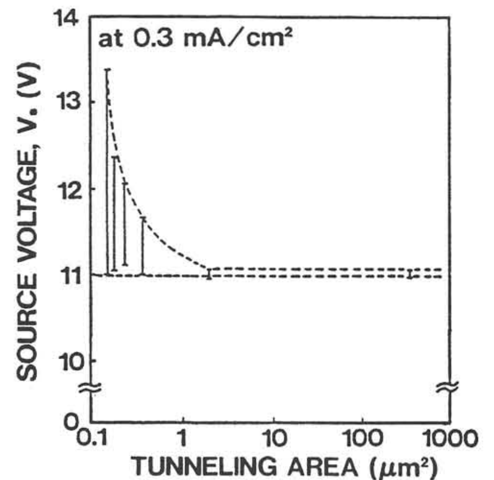


Fig.2 Relationship of voltage deviation to tunneling area

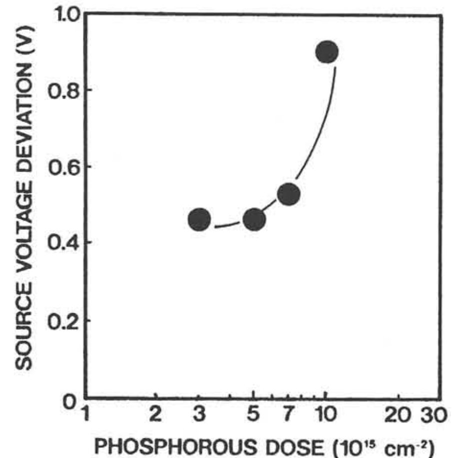
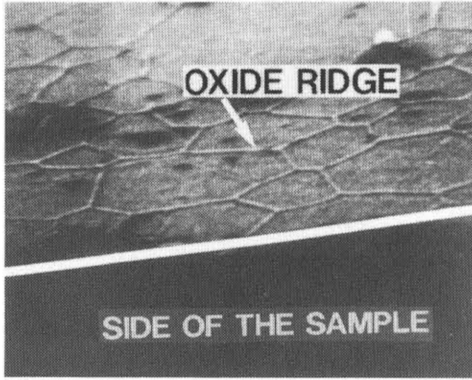


Fig.3 Relationship of P dose to voltage deviation (poly-Si thickness ; 200 nm)



100 nm

Fig.4 Bird's eye view of OXIDE RIDGE on SiO_2 surface

certain size of device is thought to have a smaller voltage deviation when the defect density gets larger. Furthermore, the smaller P density causes a smaller voltage deviation (Fig.3). These results show that P in the gate poly-Si film is the key factor to the voltage deviation.

In order to clarify how these defects are formed, the SiO_2 surface was observed by SEM after stripping the poly-Si film off the poly-Si gate MOS structure. It was found that there is a net-pattern protruding from the SiO_2 surface (dubbed an "oxide ridge" by the authors) that is not found before the gate electrode is formed (Fig.4). This pattern is inhomogeneous over the SiO_2 surface for the size of the net and the height of the ridge. For example, in a $3x10^{16}$ cm^{-2} phosphorous implanted sample annealed at 1050 °C, the ridge is about 2 nm high at its highest point, and the net is from 0.1-1 μm in radius. The Tunneling Electron Microscopic observation also shows that the oxide ridge is formed at the grain boundaries of the gate electrode poly-Si film. More importantly, an oxide ridge is highest at the triple point of grain boundaries. This inhomogeneity can lead to local deviations in gate oxide characteristics because of differences in effective oxide thickness. In other words, the total lengths

Annealing Temperature | Top view of OXIDE RIDGE 100 nm

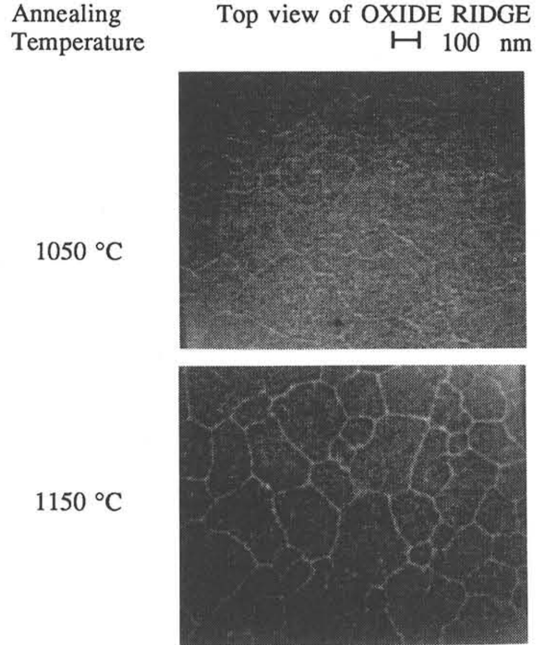


Fig.5 OXIDE RIDGE structure dependence on annealing temperature
phosphorous dose ; $1x10^{16}$ cm^{-2}
annealing time ; 60 min.

of the oxide ridges formed on each gate insulator are different from one another when the device is as small as a poly-Si grain. For example, the measured total ridge length for 0.2 μm^2 gate area distributes from 0 to 3 μm. This oxide ridge becomes smaller in radius and lower in height when the P density is lowered or the temperature after the formation of the gate poly-Si is lowered (Fig.5 and Fig.6). These two factors are closely related to the regrowth of poly-Si grains[14]. From these data, the oxide ridge is thought to be formed by the viscous flow of SiO_2 film[15] and the diffusion of P into SiO_2 film at the same time as poly-Si grain growth during high temperature processes. In addition, it was determined that a two-layer gate insulator Si_3N_4/SiO_2 film prevents the oxide ridge from growing. That is thought to be so because Si_3N_4 film obstructs the diffusion of P from the grain boundaries of the poly-Si film into the SiO_2 film.

The above results show that the smaller

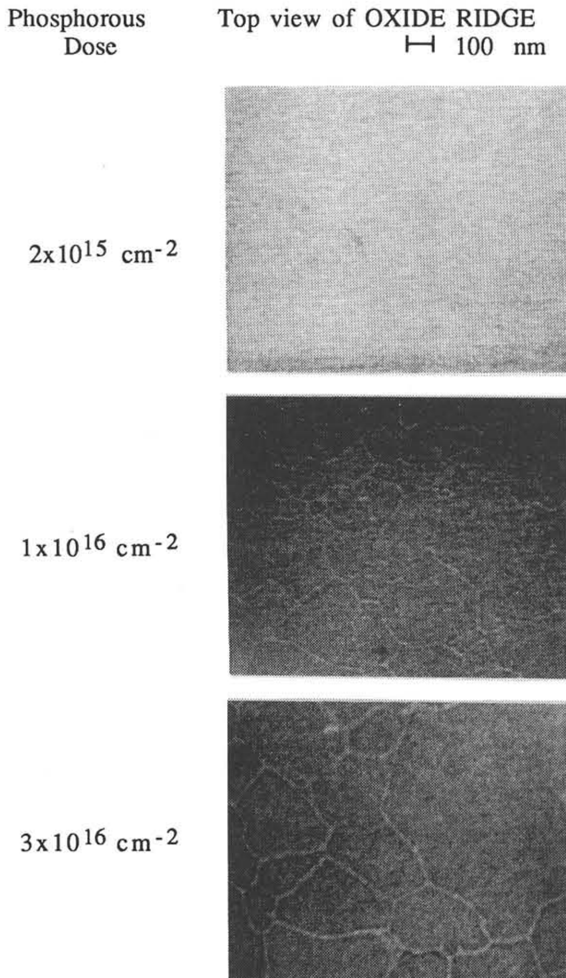


Fig.6 OXIDE RIDGE structure dependence on phosphorous dose
annealing temperature ; 1050 °C
annealing time ; 60 min.

oxide ridge makes the length of the oxide ridge included in the tunneling area be homogeneous and that the homogeneity of the oxide ridge causes the voltage deviation to be smaller. It is assumed that the defects playing a major role in the tunneling current are formed at the oxide ridge because the ridge is a P-rich layer.

Conclusions

A 1-2 nm high oxide ridge was found to appear at the gate poly-Si/gate insulator interface, which leads to the voltage deviation of the F-N tunneling current important to the write/erase performance of nonvolatile memories. It was made clear that it is necessary to restrain the reaction at the interface to reduce the voltage deviation caused in deep submicron devices. It was also determined that low-temperature processing, a low-P density for the gate poly-Si film, and a two-layer gate insulator film consisting of Si_3N_4 / SiO_2 are effective for suppressing the reaction.

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