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Effects of Depleted Poly-Si Gate on MOSFET Performance

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The electric characteristics of MOSFETs with a poly-silicon gate doped by ion implantation have been studied. It has been clarified that an inversion-layer is formed in the poly-Si gate with low impurity concentrations. This inversion in the gate has been found to have a significant influence on the MOSFET DC and AC performances. In addition, the influence of the impurity concentrations in the gate on the threshold voltage is discussed.

1.INTRODUCTION

A dual gate symmetric CMOS structure(n^+ poly-Si gate for NMOS and p^+ poly-Si gate for PMOS) is required for realizing lower sub-micron LSIs. In this dual gate CMOS the impurity concentration in the gate often becomes lower than that in a conventional gate doped by phosphorus diffusion, since the gate is normally doped by ion implantation and the annealing temperature is suppressed. Consequently, a depletion-layer is formed in the gate and causes the degradation of MOSFET performance, which has become a serious problem[1-4]. However, the influence of this depleted gate on the device characteristics has not yet been fully investigated. In this paper, the electric characteristics of MOSFETs with low impurity concentrations in the gate has been studied in detail. It has been demonstrated that the formation of an inversion-layer in the poly-Si gate significantly modulates the DC and AC performances of MOSFETs.

2. SAMPLE FABRICATION

The measured devices were conventional N-channel MOSFETs and MOS capacitors with a poly-Si gate. The doping into the poly-Si gate and the source/drain was done at the same time by As^+ ion implantation at 30 keV, followed by rapid thermal annealing (1000 °C, 20 sec.). The dose was varied from $1x10^{15}$ to $5x10^{15}$ cm^{-2}. An additional implantation was carried out in the contact region to reduce the contact resistance between the aluminum electrodes and the gate. As reference, MOSFETs with a phosphorus diffused gate were also fabricated. The thickness of the poly-Si gate and the gate oxide was 200 nm and 6 nm, respectively.

3. RESULTS AND DISCUSSION

3-1 MOSFET Performance

Figures 1 and 2 show the DC I_d-V_g and g_m-V_g characteristics in the linear region (V_d = 50 mV), respectively. Here, the As^+ implantation dose is a parameter. The threshold voltage increased monotonically with a decrease in the As dose. On the other hand, it has been observed that g_m^{max} decreased to a dose of $2x10^{15}$ cm^{-2} monotonically and increased reversely at a dose of $1x10^{15}$ cm^{-2}. In addition, double peaks in the g_m- V_g curve[3] were observed at a dose of $2x10^{15}$ cm^{-2}. It is known that depletion in the poly-Si gate causes an increase in the threshold voltage and a decrease in g_m[1- 4]. These phenomena have been so far explained by the increase in "equivalent oxide thickness" due to the formation of a depletion- layer in the gate. However, it is apparent that an increase in g_m at a dose of $1x10^{15}$ cm^{-2} and the double peaks in the g_m-V_g curve at a dose of $2x10^{15}$ cm^{-2} cannot be explained by the depletion of the gate.

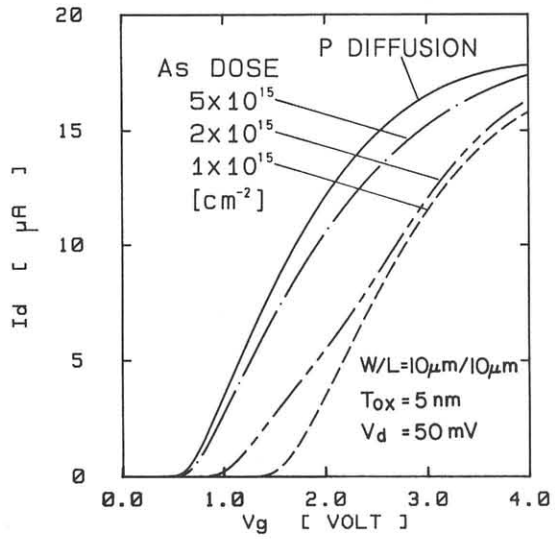

Fig.1 I_d-V_g characteristics (V_d=50 mV) as a parameter of As^+ dose

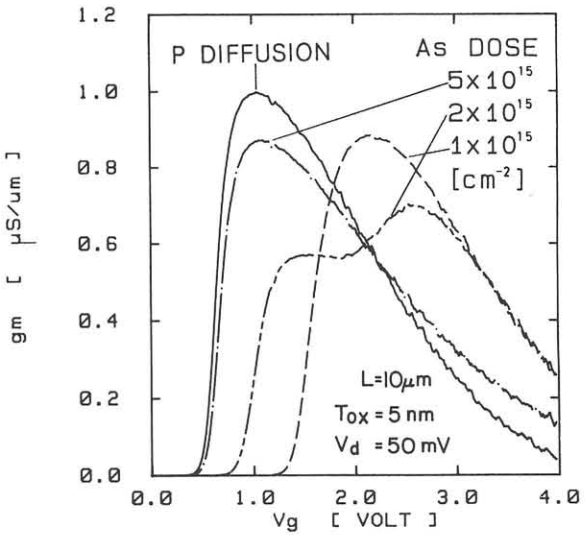

Fig.2 g_m-V_g characteristics as a parameter of As^+ dose

Moreover, a severe degradation in the pulse response time was found in the MOSFETs at lower doses. Figure 3 shows the waveforms of the source current in the linear region when a pulse voltage was applied to the gate. A long rise time (~ msec order) was clearly observed in the MOSFETs at a $1x10^{15}$ cm^{-2} dose.

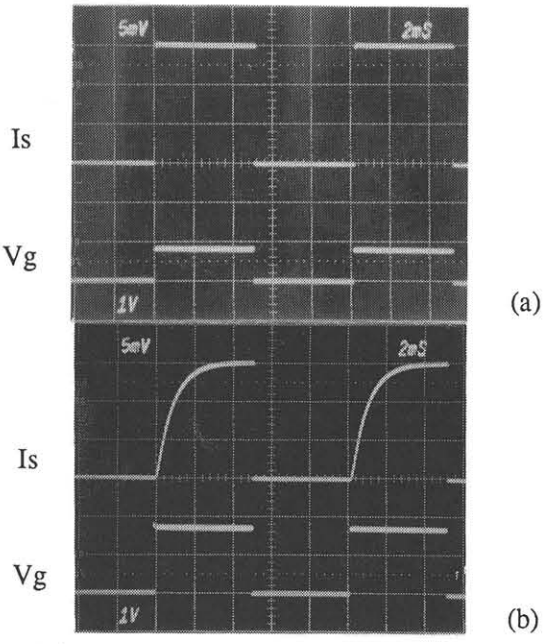

Fig.3 Source current waveforms
Dose: (a) $5x10^{15}$ (b) $1x10^{15}$ cm^{-2}

3-2 C-V Characteristics

The C-V characteristics were studied in order to clarify the cause of the above anomalous behaviors. Figure 4 shows quasi-static C-V characteristics of MOS diodes. In the inversion region, the capacitance in the intermediate voltages (~ 1.5 V) decreased with a decrease in the dose, which shows the influence of the depletion of the gate. Meanwhile, the capacitance in high gate voltages (> 3 V) increased for doses lower than $2x10^{15}$ cm^{-2}. This fact suggests that the formation of an inversion-layer in the poly-Si gate causes an increase in the capacitance[3].

Another evidence for gate inversion has been found in the C_{gc}(gate-channel capacitance) - V_g curves of MOSFETs (Fig.5). A distinct frequency dispersion of the capacitance was observed for the MOSFETs at lower doses. This phenomenon can be explained by considering that the inversion carrier cannot respond to the gate voltage at high frequency. Also, the threshold voltage for the gate inversion at a dose of $2x10^{15}$ cm^{-2} can be estimated to be ~ 2 V from Fig.5, because the frequency dispersion is considered to appear at the voltage where the inversion-layer is formed in the gate.

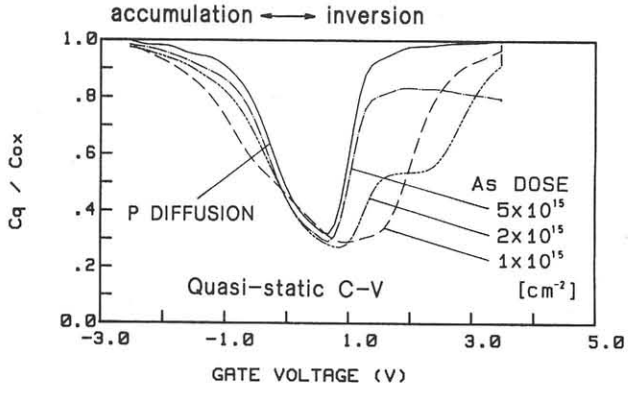

Fig.4 Quasi-static C-V characteristics as a parameter of As^+ dose

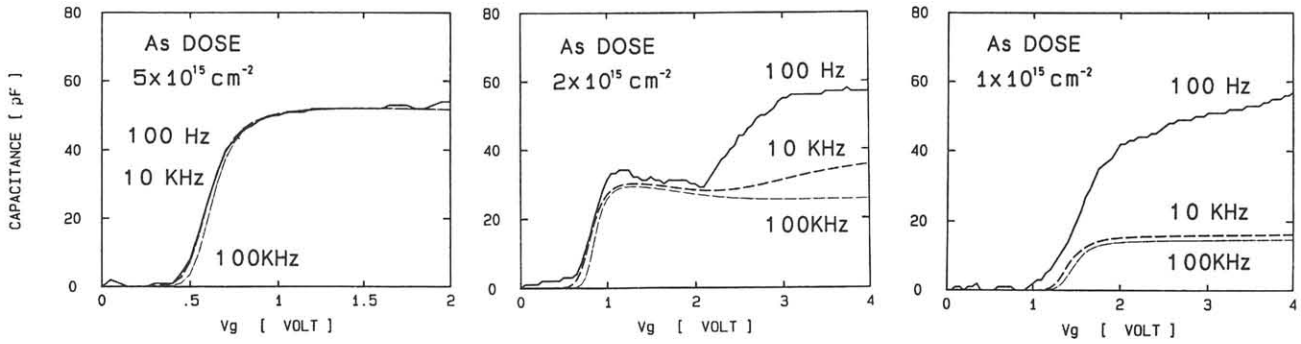

Fig.5 C_{gc}(gate-channel capacitance)-V_g characteristics as a parameter of measurement frequency.

Accordingly, the increase of g_m at a $1x10^{15}$ cm^{-2} dose can be explained by the increase in gate capacitance due to the gate inversion. In addition, this gate inversion can be responsible for the double peaks in the g_m curve for a $2x10^{15}$ cm^{-2} dose. This is because a kink in the g_m curve has been observed at the threshold voltage for the gate inversion. Furthermore, the long pulse response time in the MOSFETs at lower doses can be explained by the time delay in the generation of the inversion carrier in the gate, which is also reflected in the frequency dispersion in C_{gc} at lower doses.

3-3 Simulation Results

The DC I_d-V_g curves of the MOSFETs with lower impurity concentrations in the gate have been calculated by a 2-D device simulator in order to confirm the influence of the gate inversion (Fig.6). Here, the gate region was assumed to be single-crystal Si. The appearance of a hump and the increase in gm with lower impurity concentrations has been found to be reproduced in the simulation. A high density of holes was also observed in the gate region near the interface. These results support the above interpretation that gate inversion causes the anomalous behaviors seen in Figs.1 and 2. The formation of the depletion- and inversion-layers with increasing the gate voltage is shown in Fig.7 schematically.

3-4 Relationship between the threshold voltage and impurity concentration in the gate

In order to estimate the influence of the depletion and the inversion in the gate on the MOSFET performance more quantitatively, the relationship between the impurity concentration in the gate and the threshold voltage was calculated using a simple 1-D

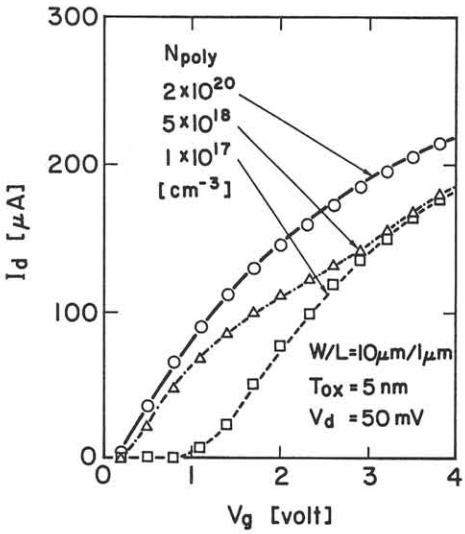

Fig.6 I_d–V_g characteristics calculated using a 2-D device simulator

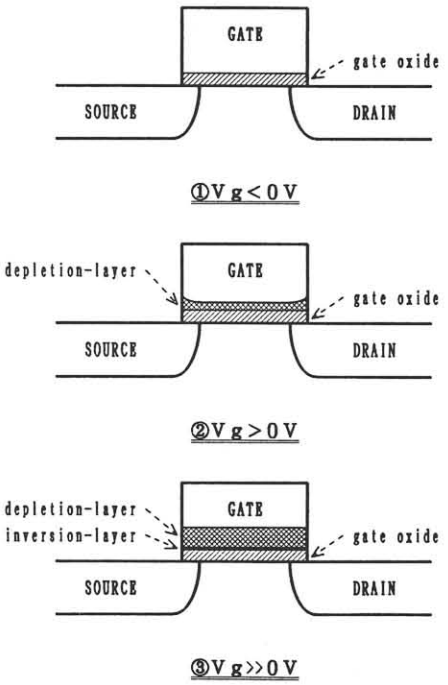

Fig.7 Schematic diagram of MOSFETs at various gate biasing voltages

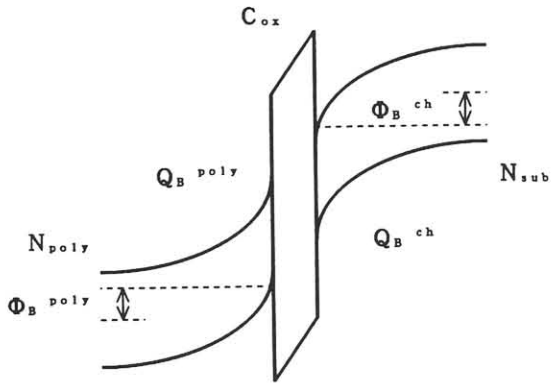

Fig.8 Band diagram of MOS structure with depleted Si gate. Here, Q_B^{ch} and Q_B^{poly} are given by the following equations:

$$Q_B^{ch} = \sqrt{4\varepsilon_{Si} q N_{sub} \phi_B^{ch}}$$

$$Q_B^{poly} = \sqrt{4\varepsilon_{Si} q N_{poly} \phi_B^{poly}}$$

model. The threshold voltage for the inversion of the channel, V_{th}^{ch}, and for the inversion of the gate, V_{th}^{poly}, can be expressed approximately by the following equations. Here, the definitions of the parameters used in the equations are given in Fig.8. In case of $N_{sub} < N_{poly}$,

$$V_{th}^{ch} = -\phi_B' + 2(1+N_{sub}/N_{poly})\phi_B^{ch} + Q_B^{ch}/C_{ox}$$

$$V_{th}^{poly} = \phi_B' + Q_B^{poly}/C_{ox}$$

In case of $N_{sub} > N_{poly}$,

$$V_{th}^{ch} = \phi_B' + Q_B^{ch}/C_{ox}$$

$$V_{th}^{poly} = -\phi_B' + 2(1+N_{poly}/N_{sub})\phi_B^{poly} + Q_B^{poly}/C_{ox}$$

Here, $\phi_B' = (\phi_B^{ch} + \phi_B^{poly})$. Figure 9 shows the calculated threshold voltages for the channel and gate inversions. Experimental threshold voltages are plotted on the calculated curves, because the electrically active impurity concentrations are unknown for individual implantation doses. As shown in Fig.9, both the experimental threshold voltages for the channel and the gate can be explained by the same impurity concentration value. This fact indicates that the above simple model used in the calculation is valid. The above relationship provides a simple guideline to evaluate the degradation in MOSFET performance for an active impurity concentration in the poly-Si gate.

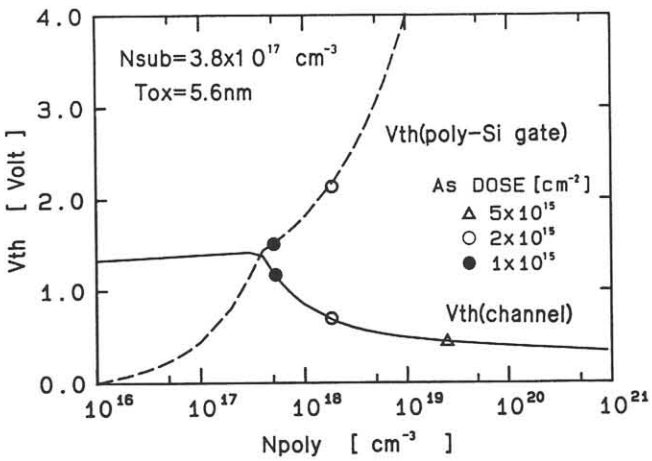

Fig.9 Relationship between gate impurity concentration and threshold voltages of channel and gate

4.CONCLUSION

The effects of a poly-Si gate with low impurity concentrations on MOSFET performance have been studied. It has been clarified that an inversion-layer is formed in the poly-Si gate under the condition that the impurity concentrations in the gate are lower and/or the gate voltage is higher. This inversion in the gate has been found to have a significant influence on the MOSFET DC and AC performances.

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