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Mechanical Stress Induced Threshold Voltage Shifts for Nitrided Oxide Gate n^- and p^- MOSFETs

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Short-channel effects on threshold voltage were evaluated in nitrided oxide n- and p-MOSFETs. It was found that some nitrided oxide n-MOSFETs show reduced threshold voltage, compared with that for a very long channel transistor, even when the channel length is 4μm, while such effect was found to be small in the p-MOSFET case. The effect is probably explained by the interface states caused by mechanical stress in the nitrided oxide gate samples.

INTRODUCTION

The rapid thermal nitridation (RTN) technique has been applied to gate oxide formation in MOSFETs [1-5]. Recently, an interesting effect that nitrided oxide films have on mobility in n- and p-MOSFETs was reported [2,3,5], where the mobility in a nitrided oxide gate n-MOSFET under high gate bias is higher than that in the pure oxide gate, while the mobility in a nitrided gate p-MOSFET is lower. An explanation for this strange phenomenon has been proposed [5], suggesting that nitrided oxide induces tensile stress, which increases n-MOSFET mobility and makes p-MOSFET mobility lower. In this paper, a new MOS short-channel effect peculiar to nitrided oxide gate MOSFETs is reported. The paper shows that this effect is also probably caused by mechanical stress.

EXPERIMENTS AND RESULTS

N- (n^+ poly gate) and p- (p^+ poly gate) MOSFETs with both nitrided oxide gates and pure oxide gates were fabricated. In some samples, nitridation was accomplished by RTN (Rapid Thermal Nitridation) after gate oxide formation. In some samples, nitride film was deposited by LPCVD. Sample fabrication conditions are listed in Table 1.

Figure 1 shows the n-MOSFET threshold voltage dependence on effective channel length. Threshold voltages for the "stacked nitridation" samples were larger than those for the "pure oxide" samples, due to negative charges in the stacked nitride films. On the contrary, threshold voltages for the "rapid nitridation" samples were smaller, due to positive charges. In the n-MOS case, some of the nitrided oxide n-MOSFETs show reduced threshold voltage, even when L_{eff} is 4 μm, compared with that at L_{eff} = 10 μm. This phenomenon appears for both the "rapid nitridation" and "stacked nitridation" samples. The threshold voltage reduction in nitrided gate n-MOSFETs may be explained by donor layer formation due to nitrogen diffusion into the substrate [3]. The donor layer changes a surface channel n-MOSFET into a buried channel n-MOSFET. It is known that threshold voltage reduction is significant in a buried channel MOSFET. P^+ poly-gate buried-channel n-MOSFETs with an arsenic implanted layer were fabricated, and the short channel effects were measured and plotted (Fig.1). It

Table 1. Sample fabrication conditions

	SAMPLE FABRICATION PROCESS			T_{OX} (C-V)	N CONC. AT Si/SiO_2 INTERFACE
	FURNACE OXIDATION	NITRIDATION	RE-OXIDATION		
PURE OXIDE	10 nm	–	–	10.8 nm	0%
RTN RAPID NITRIDATION a	10 nm	1200°C	1200°C	10.9 nm	8.3%
b		1000	1000	10.9	2.8
c		RTN 900	RTO 900	11.1	2.0
d		1200	1000	10.5	8.4
e		1200	900	10.4	9.8
SN STACKED NITRIDATION	–	LPCVD Si_3N_4 6 nm	FURNACE OXIDATION	6.0	?

should be noted that, when L_{eff} was 4 μm, no threshold voltage reduction was observed from the threshold voltage for the 10 μm n-MOSFET. In the pure gate oxide case, when the source and drain junction depths were about 0.2 μm, as in this case, no threshold voltage reduction was usually observed, at L_{eff} = 4 μm, from the threshold voltage at L_{eff} = 10 μm, even in a buried channel device. Usually, the threshold voltage reduction in the buried channel MOSFETs becomes larger than that in the surface channel MOSFETs, in submicron channel length range.

Nitrogen SIMS profiles in the Si substrate were obtained, as shown in Fig.2. Very little difference in the nitrogen diffusion into the Si substrate was observed, between the nitrided oxide gate sample and a plain Si sample. Thus, the significant threshold voltage reduction in nitrided oxide gate n-MOSFETs cannot be explained by the donor layer formation.

Figure 3 shows the threshold voltage reduction dependence on the re-oxidation temperature. It should be noted that, when the re-oxidation temperature is higher, the threshold voltage reduction at L_{eff} = 4 μm, from the threshold voltage at L_{eff} = 10 μm, becomes less pronounced. Donor layer formation, due to nitrogen diffusion, cannot explain this phenomenon, because in high temperature, the nitrogen diffusion becomes large, and the buried layer becomes large. The threshold voltage shift behavior in Fig.3 would be explained by mechanical stress, as in the mobility case [5]. High temperature re-oxidation will relax stress at the silicon oxide interface.

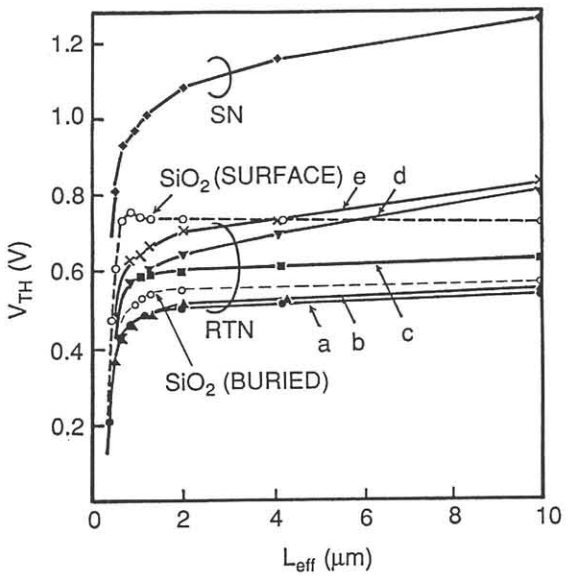

Fig 1. V_{th} dependence on L_{eff} for several surface channel n-MOSFETs with RTN and SN gate oxide.

Figure 4 compares the threshold voltage dependence on channel length, with the stress dependence reported by Hamada et. al. [6]. Stress reduced with decrease in the channel length. Threshold voltage reduction dependences are very similar to that for

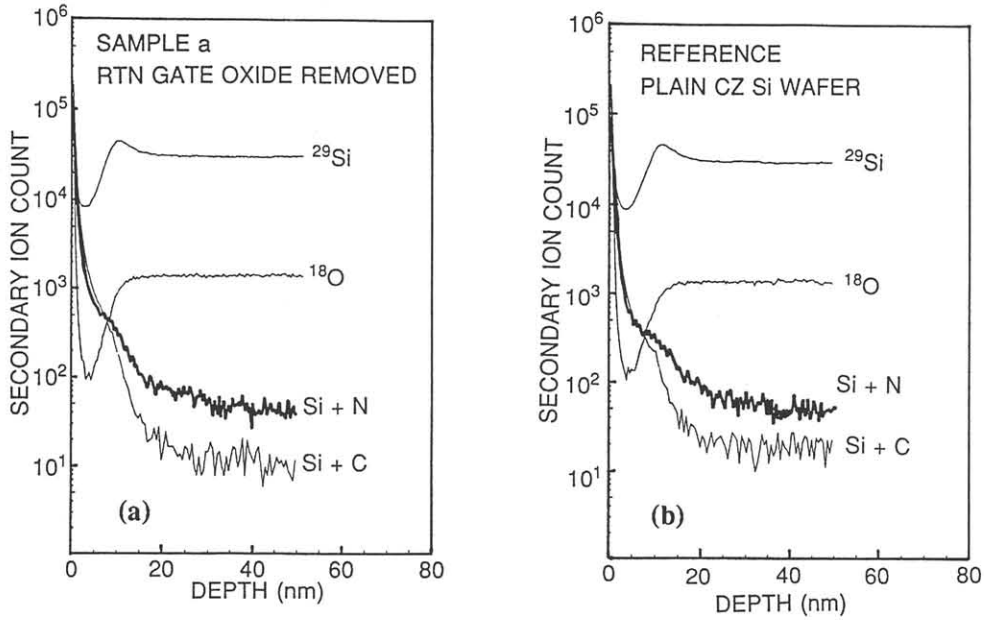

Fig 2. Si, O, N, C profiles measured by SIMS ($^{18}O_2^+$ source)
(a) RTN sample: gate oxide removed
(b) Reference: plain Cz-Si Wafer

the stress reduction, which further suggests that stress is the reason for the unusual short-channel effects. Figure 5 shows the p-MOSFET threshold voltage dependence on the effective channel length. Contrary to the n-MOSFET case, no threshold voltage reduction, from that at L_{eff} = 10 μm, was observed at L_{eff} = 4 μm.

From these results, it is estimated that the unusual short channel effect is caused by interface states, which are generated by mechanical stress in the fabrication process, as shown in Fig.6. The stress-induced interface states are significant in the long channel case, especially for L_{eff} = 10 μm. The n-MOSFET threshold voltage becomes larger at L_{eff} = 10 μm than that at L_{eff} = 4 μm, because most of the stress-induced interface states, peculiar to the long channel MOSFET, are negatively charged at the threshold bias (Fig.6(a)). The p-MOSFET threshold voltages are not so different, between at L_{eff} = 10 μm and at L_{eff} = 4 μm, because most of the stress-induced interface states are neutral at the threshold bias for the p-MOSFET case (Fig.6(b)).

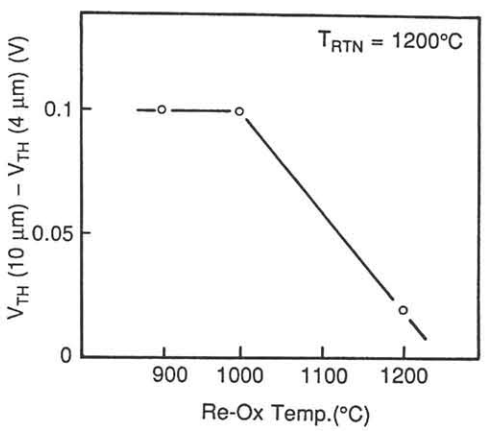

Fig 3. Dependence of n-MOSFET V_{th} shift, between L_{eff} = 10 μm and L_{eff} = 4μm, on re-oxidation temperature.

CONCLUSION

Short-channel effects on threshold voltage were evaluated in nitrided oxide n- and p-MOSFETs.

For some nitrided oxide n-MOSFETs, threshold voltages for relatively long channel devices reduced from those for very long channel devices.

For the nitrided oxide p-MOSFET case, the effect was found to be very small.

The effect is probably explained by the interface states caused by mechanical stress in the nitrided oxide gate samples.

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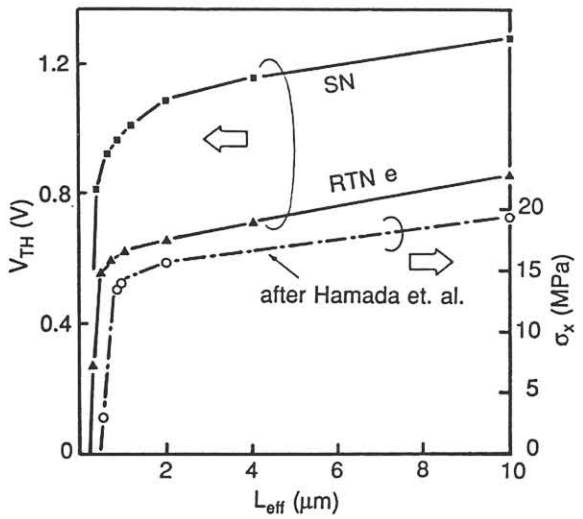

Fig 4. Comparison between n-MOSFET V_{th} and σ_x (mechanical strain) dependences on L_{eff}.

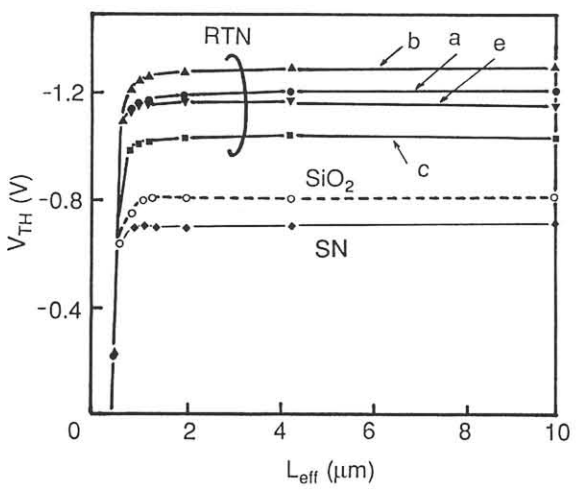

Fig 5. V_{th} dependence on L_{eff} for several surface channel p-MOSFETs with RTN and SN gate oxide.

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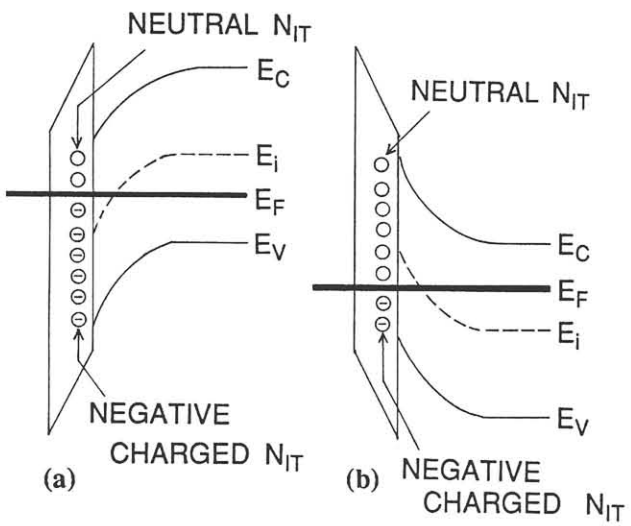

Fig 6. Estimated energy distribution for the additional interface states, possibly induced by mechanical stress in long channel (L_{eff} = 10 μm) MOSFETs.
(a) n-MOSFET case: Most of the stress-induced interface states are negatively charged in the inversion bias region.
(b) p-MOSFET case: Most of the stress induced-interface states are neutral in the inversion bias region.