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Hot-Carrier Degradation Mode and Prediction Method of DC Lifetime in Deep-Submicron PMOSFET

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Hot-carrier-induced device degradation is investigated for quarter-micron level burried-channel PMOSFETs with extremely shallow source/drain junctions (80 nm) and ultra-thin gate oxide (3.5 nm). It is found that the hot-carrier degradation mode for these small devices is quite different from previous reports. The new degradation mode is caused by interface-traps generated by hot hole injection into the gate oxide near the drain. The DC device lifetime for the new mode can be predicted from the substrate current, but not gate current.

1. INTRODUCTION

Hot-carrier reliability is one limiting factor in scaling down devices to deep submicrometer [1]. At this size, hot carriers will cause problems in PMOSFETs as well as NMOSFETs. Up to now, most work on burried-channel(BC) and surface-channel(SC) PMOSFETs has concentrated on half- to one-micron gate lengths[2]-[9]. The main cause of the degradation in these devices is trapped electrons injected into the gate oxide, and the device lifetime has been evaluated using gate current or substrate current.

This paper studies hot-carrier-induced device degradation for a quarter-micron level BC-PMOSFET. A newly-observed degradation mode, its cause, and the method of predicting the device lifetime will be described.

2. DEVICE FABRICATION

The quarter-micron level BC-PMOSFETs used in this study were fabricated by an N^+ poly-Si gate process using electron beam lithography. The gate oxide thickness is 3.5 nm, and the source/drain junction depth is 80 nm. BF_2 implantation to adjust threshold voltage, and relatively deep arsenic and phosphorus implantation to prevent punchthrough were performed through a temporary oxide. After etching off the oxide, the gate oxide was grown in dry O_2 at 800°C. The extremely shallow junctions were obtained using low-energy BF_2 implantation (15 keV) after pre-amorphization by silicon implantation and rapid thermal annealing[10]. No passivation film was used.

3. RESULTS AND DISCUSSION

3.1. NEW DEGRADATION MODE

It is known that the maximum device degradation in BC-PMOSFETs is observed at a stress bias condition showing the maximum gate current in the saturation region. The gate current is caused by electrons being injected into the gate oxide near the drain and reaching the gate electrode. The degradation is caused by the effective channel-length reduction due to the trapped electrons in the oxide near the drain[5]. As a result, transconductance g_m and threshold voltage V_T increase after stressing. On the other hand, for SC-PMOSFETs, the maximum degradation appears at a stress

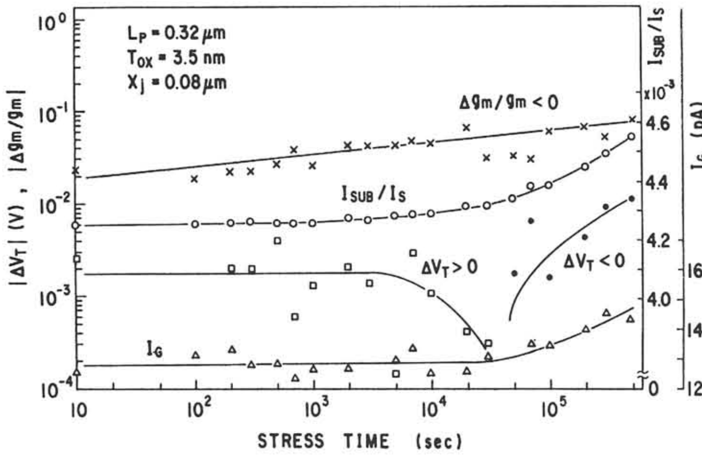

Fig.1 Changes in $\Delta g_m/g_m$, ΔV_T, I_{SUB}/I_S and I_G during stressing at V_D=-3.5 V and V_G= -1.6 V.

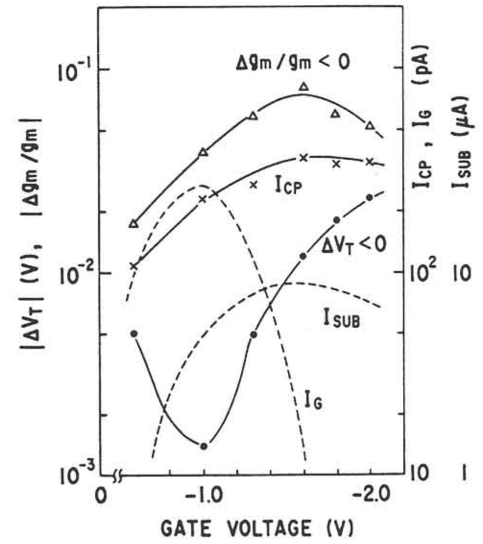

Fig.2 Relationships between device degradation ($\Delta g_m/g_m$, ΔV_T, I_{cp}) and stress gate voltage, with I_{SUB} and I_G dependences upon gate voltage. Stress drain voltage is fixed at -3.5 V, and stress time is $5x10^5$ sec.

condition showing the maximum substrate current but not the maximum gate current[6]. Nevertheless, the degradation also increases g_m and V_T, as with the BC. Therefore, the degradation of SC-PMOSFETs is also due to the trapped electrons[9].

Changes in $\Delta g_m/g_m$, ΔV_T, the ratio of substrate current to source current I_{SUB}/I_S, and gate current I_G during stressing for a quarter-micron level BC-PMOSFET are shown in Fig.1. Stress bias condition was selected in the saturation region. The figure shows that g_m decreases ($\Delta g_m/g_m$<0) and V_T initially increases slightly(ΔV_T>0), then turns negative (ΔV_T<0). These tendencies are completely contrary to the previous literature. Moreover, I_{SUB}/I_S and I_G increase with time, which suggests positive charge generation in the oxide[4].

The effects of stress gate voltage on ΔV_T, $\Delta g_m/g_m$ and charge pumping current I_{cp} are shown in Fig.2 along with I_{SUB} and I_G dependences upon gate voltage V_G. I_{cp} is proportional to the amount of interface traps generated by hot carrier injection [11]. The curve of $\Delta g_m/g_m$ vs. stress gate voltage corresponds to I_{SUB} vs. V_G but not to I_G vs. V_G, which means that the g_m degradation is caused by hot hole injection but not hot electron injection. In addition, the fact that $\Delta g_m/g_m$ changes with I_{cp} means that g_m degradation is due to generated interface traps.

Therefore, the newly-observed degradation mode in the saturation region is considered to be caused by interface traps generated by hot hole injection.

3.2. VERIFICATION OF INTERFACE-TRAP EFFECT

It is known that interface traps in the upper part of the energy gap are acceptor-like, and traps in the lower part are donor-like[12]. For PMOSFETs under inversion condition, donor-like interface traps between the quasi-Fermi level and the middle of the gap can be positively charged, as shown in Fig.3. The amount of the charged traps increases with increasing $|V_G|$. If the newly-observed degradation mode is due to generated interface traps, the effect of V_G on the amount of charged traps should appear in the device characteristics. V_G dependences upon source

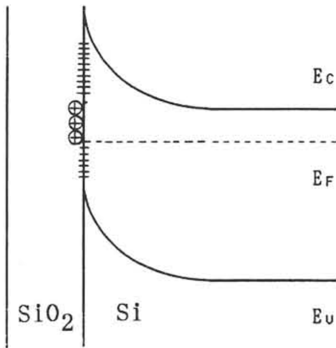

Fig.3 Positively-charged donor-type interface traps in PMOSFETs under inversion condition.

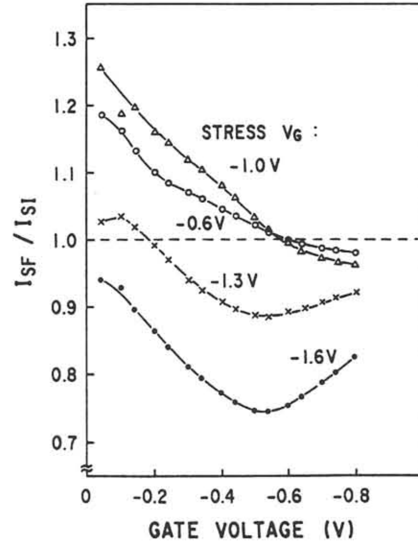

Fig.4 Source current ratio (I_{SF}/I_{SI}) as a function of gate voltage with stress gate voltage as a parameter. Stress drain voltage is -3.5 V. Stress time is $5x10^5$ sec.

current ratio of I_{SF}/I_{SI} at V_D=-0.05V are shown in Fig.4 with stress gate voltage as a parameter. I_{SI} and I_{SF} are I_S before and after stressing. $I_{SF}/I_{SI}>1$ means an increase in I_S due to stressing. The figure shows that $I_{SF}/I_{SI}>1$ for small $|V_G|$ (subthreshold region) in the stress gate-voltage range of -0.6~-1.3 V. The increase in I_S is due to the trapped electrons. However, with increasing $|V_G|$, I_{SF}/I_{SI} becomes less than one. This is because the amount of the positively-charged interface traps becomes larger than the amount of trapped electrons. The stress gate-voltage range of -0.6~-1.3 V, where the effect of the trapped electrons is significant, corresponds well to the V_G range of high I_G due to hot electron injection in Fig.2.

It is therefore concluded that the new degradation mode in the saturation region is caused by hot-hole-induced interface traps. Significant hot-hole injection results from the increase in hole injection rate due to the decrease in the depth of the hole current path near the drain. Such an increase in hot-hole injection rate must be more significant in SC-PMOSFETs. Therefore, the new degradation mode will be very important in future PMOSFETs, including the SC-type. In fact, trapped holes and generated interface traps have been detected under particular bias conditions even in 1-um-level SC-PMOSFETs, but in that case the main cause of degradation is trapped electrons[8].

3.3. LIFETIME PREDICTION METHOD

Although the device lifetime is usually predicted from gate current or substrate current[7,9], the prediction method needs to be reconsidered for the new degradation mode. DC device lifetime is shown as a function of I_G per unit channel width W_{eff} in Fig.5, where the lifetime is defined as the time required to reach ΔV_T=10 mV. The relationship is not linear on a log-log scale, therefore I_G cannot be used as a lifetime predictor.

The relationship between the lifetime τ and I_{SUB}/W_{eff} is shown in Fig.6 for I_{SUBMAX}-bias and $V_D=V_G$ stress conditions. The relationship $\tau \propto (I_{SUB}/W_{eff})^{-1.7}$ is obtained for both stress conditions. Therefore, substrate current can be used as a lifetime predictor for the new degradation mode.

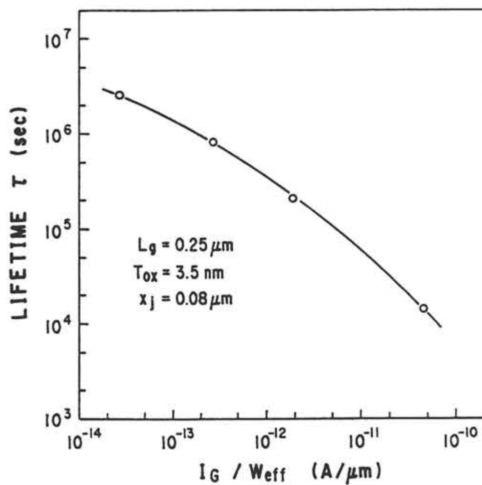

Fig.5 DC device lifetime as a function of gate current per unit channel width. Stress bias condition is I_{SUBMAX} (stress V_D=-3.0~ -3.8 V).

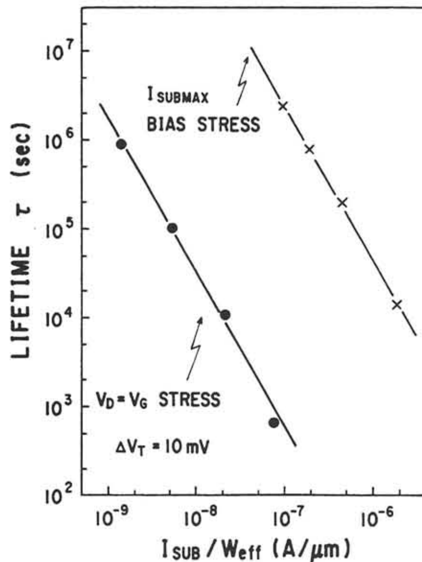

Fig.6 Relationship between DC device lifetime and substrate current per unit channel width for I_{SUBMAX}-bias (stress V_D= -3.0~ -3.8 V) and V_D=V_G (=-2.85~ -3.8 V) stress conditions.

4. CONCLUSIONS

A new hot-carrier degradation mode was observed in quarter-micron level BC-PMOSFETs. The new mode is caused by interface traps generated by hot hole injection. The DC device lifetime for the new mode can be predicted from substrate current, but not gate current. The new degradation mode will be very important in future PMOSFETs, including SC-PMOSFETs.

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