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Hot-Carrier Degradation Effects Relevant in Real Operation of MOSFETs

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In this paper various stages appearing in digital logic, such as inverters, NANDs, NORs, and transfer gates are hot-carrier stressed. Transient effects are proven to be unimportant while the effect of voltage combinations can cause small errors in duty cycle calculations. Furthermore, a relation between static and dynamic lifetimes is given and a more realistic lifetime criterion is proposed.

1. INTRODUCTION

In the past ten years, great efforts have been devoted to gaining an understanding of hot-carrier degradation effects. A picture has evolved in which the combined injection of electrons and holes can explain the experimental data found in n-MOSFETs, while injected electrons are found to be responsible in p-MOSFETs. It is now time to introduce this knowledge into applications and to discuss the practically relevant effects. This issue is especially important, as reliability assurance against hot-carrier degradation is becoming an increasing problem in VLSI. In this paper, different operating modes of the kind appearing in logic applications are investigated with respect to hot-carrier degradation and a worst case duty cycle estimation for application in hot-carrier reliability assurance is given. Furthermore, we present results relating to a more realistic lifetime criterion. We used devices with l_G = 0.8μm and t_{ox} = 16nm from a CMOS process with LDD for the n-channel only.

2. TRANSIENT EFFECTS

When static and dynamic stresses are compared, the question of transient effects arises. For sufficiently controlled stressing pulses[1], we expect the appearance of intrinsic nonstationary effects only for transients below a few hundred picoseconds[2]. However, the effects of fast interface states cannot be so easily excluded, so that we investigate these effects for transients down to 0.5ns in this paper. Our results prove clearly that by using an appropriate duty cycle calculation[3], the static and dynamic results agree and that no transient effects are present in the n-channel MOSFET's of the wafers used (see Fig. 1). A similar investigation in p-MOSFET's is not so simple, as the degradation alters the injected currents by a large amount. There are, however, clear hints that transient effects do not exist in p-MOSFET's either. These considerations allow the duty cycles of MOSFET's in circuits to be calculated.

3. STRESS MEASUREMENTS OF LOGIC STAGES

3.1 Inverter chain with varying input pulses of subsequent stages

An inverter chain was designed so that the channel width of each subsequent stage increased by a factor of three. An external stress pulse train was applied with a slope of 1ns which decreased to about 300ps in the last stage. This caused a decreasing overlap

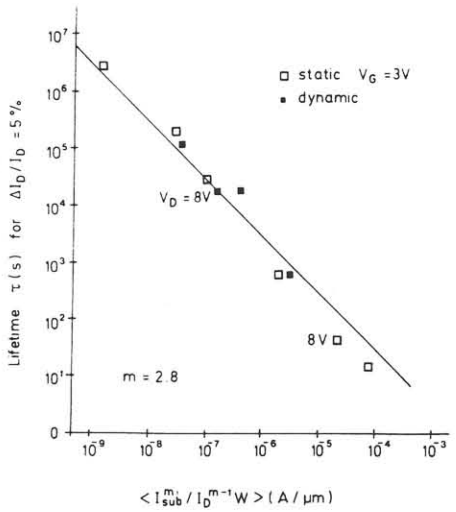

Fig. 1 Lifetime τ vs. time average of I_{sub}^m/I_D^{m-1}, the value of m being determined by a separate plot $\tau(I_{sub})$ for constant I_D which is not shown here.

of the gate and drain voltage transients of subsequent stages and a decreasing hot-carrier-related duty cycle. Each device (n- and p-channel) in the inverter chain could be independently characterized. In Fig. 2, the n-channel results of a stress with an input stress pulse amplitude of 8V are shown, clearly monitoring the decreasing duty cycle (analogous results being obtained for the p-MOSFET). The effect of different realistic loads is, however, relatively moderate, leading to a range in lifetimes of a factor of only four.

3.2 Inverters with voltage overshoots

A second inverter chain was designed so that each inverter had to drive a load a third as great as its own. This was achieved by decreasing the width of subsequent stages by the same factor. This reduced load is known to cause voltage overshoots with increasing magnitude for stages with higher numbers. Fig. 3 depicts the n-channel stress results. These show a somewhat increased degradation from the overshoot-induced higher stress voltages. A check was made to ensure that this result was not influenced by width-dependent degradation effects.

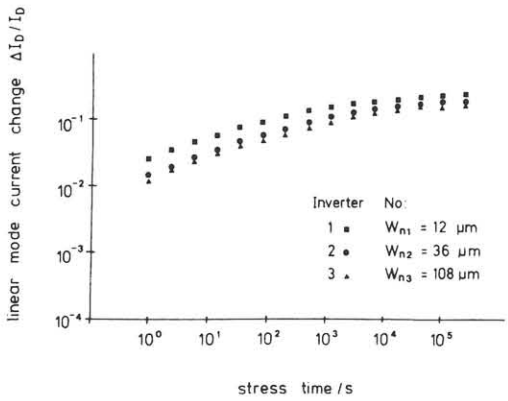

Fig. 2 Degradation vs. stress time for n-MOSFETs in an inverter chain with decreasing transients, decreasing duty cycle and thus decreasing degradation

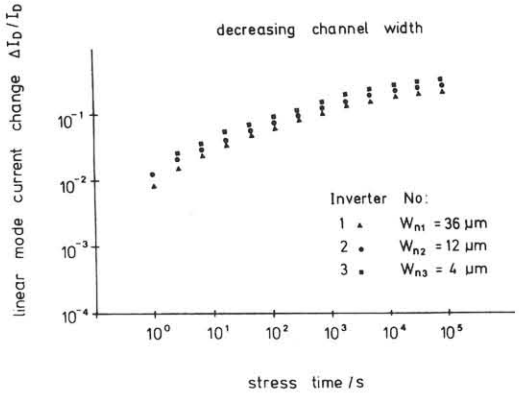

Fig. 3 Increased degradation due to overshoots in low-load inverter chains

3.3 NAND/NOR-type inverters

The worst case in NANDs and NORs is approximated by an inverter-type structure, which is characterized by altered width dimensions as compared to a standard inverter. In the NAND/NOR, the p/n-MOSFET has an unusually small width. Its response is slower and the next stage, a normally dimensioned inverter, receives a slower rising/falling input slope. Duty cycle calculations show that the degradation of a MOSFET in an inverter environment is controlled much more by the gate voltage slope than by the drain voltage slope. Thus the p/n-MOSFET with reduced width has quite a usual degradation while the n/p-MOSFET in the next stage shows a somewhat increased degradation compared to that in the NAND/NOR-type stage. The NAND result is shown in Fig.

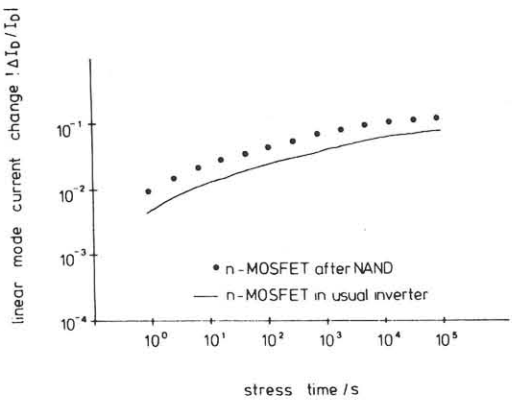

Fig. 4 Increased degradation of the n-channel MOSFET in the inverter following the NAND-type circuit

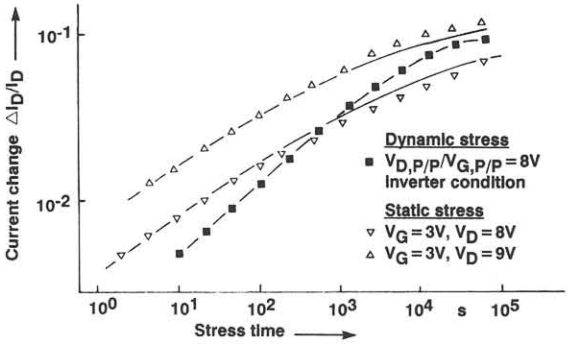

Fig. 5 Different time behaviours of dynamic and static degradation caused by different injection conditions in another process

4, demonstrating the increased degradation of the n-MOSFET in an inverter after the NAND. The result of the NOR is analogous.

In all cases an agreement with the above duty cycle calculation was confirmed. Furthermore it is emphasized that the differences between the degradation of an ordinary inverter and the specific applications are rather small leading to differences in lifetimes of about a factor of only four.

4. THE EFFECT OF COMBINATIONS OF GATE AND DRAIN VOLTAGES

In the following, we examine the effect of different combinations of gate and drain voltages[4]. Under static stress, there exists only a single injection condition, at least for small amounts of degradation. During dynamic stress, however, different combinations of stressing voltages occur, which lead to noticeable effects in the degradation of the n-MOSFETs. At low gate and high drain voltages during stress, we observe the trapping of fixed positive charges, together with the formation of interface states. The interface states are uncharged in this condition (pinch-off) and the positive charge causes a decrease of the electric field, as proven by substrate current measurements. Only in a dynamic stress is this positive charge neutralized by the injection of electrons at high V_G, so that the electric field reduction does not occur. This leads to a somewhat enhanced degradation in dynamic cases (Fig. 5). The effect is variously pronounced in different technologies and reduces the lifetime by up to an order of magnitude (in the process used in Figs. 1-4, 6-8, the effect is less pronounced). It can complicate comparisons of static and dynamic stress results, providing an argument for duty cycle calculations to be cross-checked with dynamic stress tests.

5. ESTIMATION OF A DYNAMIC DUTY CYCLE

From the experimental data in Fig. 1 (8V results) we can evaluate the ratio between a typical dynamic and static lifetime to be 0.25 % for a cycle time of 40ns. Note that this estimation is not based on the duty cycle calculation but is purely experimental. On the basis of the investigation of the logic stages (see chapter 3, above) a worst-case duty cycle of 1% is estimated for the n-channel MOSFET and even less for the p-MOSFET. This holds good on the assumptions that subsequent stages are not allowed to differ by more than a factor of three in their current driveability. This limitation is in any case rather common as a design rule for maximum circuit speed.

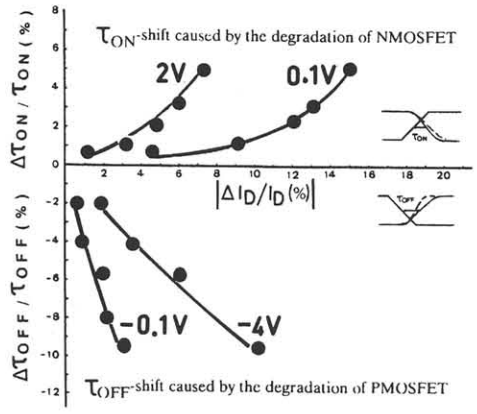

Fig. 6 Contribution of n-MOS and p-MOS degradation to delay shift. Transistor characterization is performed at $|V_G|=5V$ and V_D as given in the figure.

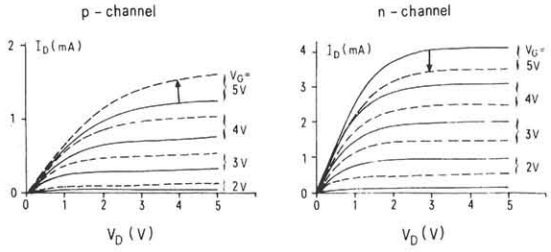

Fig. 7 The degradation of the normal-mode output characteristics after transmission gate stress in an n- and p-channel MOSFET. Due to the degradation at drain and source, the current change looks essentially homogeneous.

During operation, different voltage conditions occur. While in the linear mode usually monitored, the electron Fermi level in the damaged region of the n-MOSFET is close to the conduction band, under pinch-off conditions it is located deeper in the bandgap. There, part of the interface states are uncharged, which leads to a reduced current drift. On this basis, we introduce a more realistic lifetime criterion which leads to a further relaxation of hot-carrier related lifetime requirements (Fig. 6, upper part). A similar investigation in the p-MOSFET leads, however, to an aggravation (Fig. 6, lower part). This fact provides an argument for quality assurance of a process development in an advanced state on the basis of direct measurements of stage delay degradations (cf. the measurement of frequency shifts in ring oscillators in [5]).

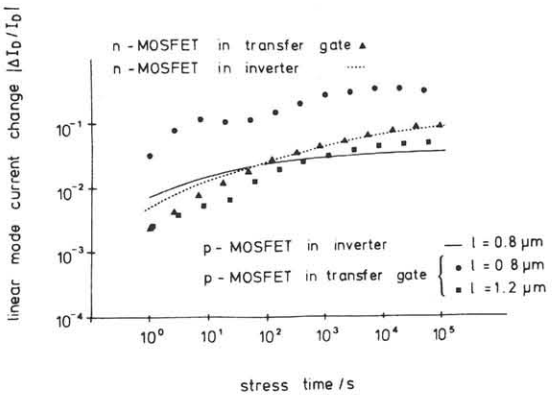

Fig. 8 Linear-mode drain current degradation of n- and p-MOSFET in a transfer gate, each compared with inverter results

6. TRANSMISSION GATE

The transmission gate is an important special case in various applications. Source and drain are alternately switched into the high state, and as a consequence the degradation takes place in both regions. The degradation of the output characteristics differs from the usual case of a stress on one side only (Fig. 7). In the case of the p-MOSFET, this leads to a greatly enhanced reduction of the effective channel length and thus to linear-mode degradation[6] (Fig. 8, full line and dots). A 0.4µm longer p-channel is required in order to compensate for this effect (Fig. 8, squares). In contrast, the linear-mode drain current degradation of the n-channel is not increased, as no degradation-enhancing effects are present here. Furthermore, this parameter is equally sensitive to damage at both source and drain. It thus represents a worst case (Fig. 8, dotted lines and triangles).

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