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A New Hot-Electron-Induced Threshold Voltage Degradation Model for nMOSFET's

Bang ZHOU and Gang RUAN

Microelectronics Institute
Fudan University
Shanghai, 200433, P. R. China

Based on the mechanism that hot-electron injected and trapped in the gate-oxide region is the main cause of the parameters degradation for short-channel nMOSFET's, a new threshold voltage degradation model is derived, in which, the nagative feedback effect of trapped electron is included, and the saturation trend of degradation is predicted.

1. INTRODUCTION

Hot-electron-induced nMOSFET's degradation has been thought to be due to hot electron trapped in the gate oxide and/or Si-SiO_2 interface-trap generation [1-7]. However, in recent works, it has been shown that the trapped electron in the gate oxide near the drain is the main cause for nMOSFET's degradation [8,9]. Trapped electron induces degradation of some important parameters, such as threshold voltage, transconductance and subthreshold slope, for nMOSFET's. In general, the relationship between threshold voltage degradation ΔV_T and stress time t is empirically fitted to $\Delta V_T \sim t^n$ (n=0.5$\sim$0.75) [1],[6]. In our paper, a new formula for the relationship between threshold voltage shift ΔV_T and stress time t is derived, which based on the mechanism that hot-electron injected and trapped in the gate-oxide region is the main cause of the parameters degradation for short-channel nMOSFET's. The good agreement between calculated results from our model and experiment data shows that the preceding model is correct. Furthermore, our model include the nagative feedback effect of trapped electron and can indicate the saturation trend of the nMOSFET's degradation.

2. PHYSICAL MODEL

In short channel nMOSFET's, there is a high and narrow electric field in the channel region near the drain [10]. Fig.1 shows the lateral electric field distribution along Silicon surface simulated by FUMOS [11] (Fudan University MOSFET Simulator). Carriers in this high field region can be accelerated into high energy and some of them can be injected into the gate oxide. Although the distribution of hot electron has a high energy tail, the distribution of hot-electron in the channel can be approximated by Boltzman distribution with electron temperature T_e higher than lattice temperature T_o. The electron density with energy ranging from E to E+dE is given by :

$$dn = \frac{4\pi(2m^*)^{3/2}}{h^3}\sqrt{E-E_c} \cdot \exp\left(-\frac{E_c-E_{Fn}}{KT_e}\right)\exp\left(-\frac{E-E_c}{KT_e}\right)dE \qquad (1)$$

where T_e is electron temperature, it can be modeled as a function of lateral electric field in channel [12].

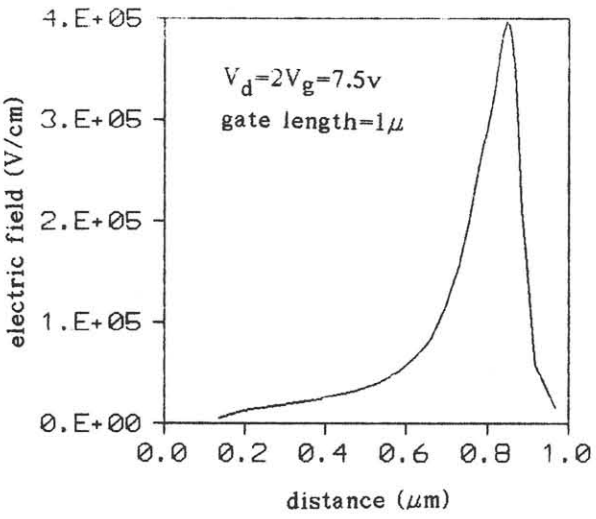

Fig.1 Lateral electric field distribution along Si surface, simulated by FUMOS

The distribution of electric field in the gate oxide of nMOSFET's is shown in Fig.2.

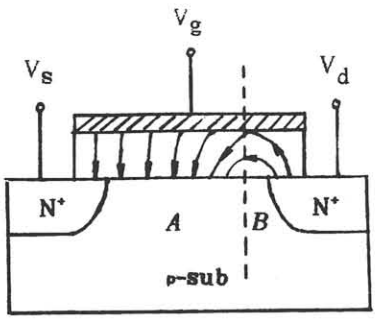

Fig.2 Electric field distribution in gate oxide at general bias condition (V_d>V_g>0)

The direction of oxide electric field in region B is opposite to that in region A. Hot electrons injected in the oxide of region A will be accelerated to gate. Hot electrons injected in region *B* will lose their energy and some of them will trap in oxide traps to be trapped charge, while the others devote to the gate current, see Fig.3. Some oxide traps are intrinsic and others are generated by injected carriers.

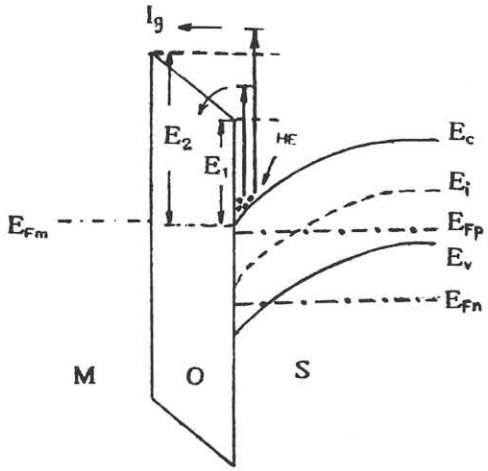

Fig.3 energy band diagram for region B

Electrons with energy higher than E_2 have chance to be injected into oxide, only those electrons with energy ranging in E_1 and E_2 will lose all their energy and trap in oxide traps to be the nagative trapped charge. The increasing rate of trapped electron number in oxide is equal to the number of electrons in channel, moving toward Si-SiO_2 interface with energy ranging from E_2 to E_1 :

$$\frac{dQ}{dt}=-\eta\frac{4\pi m^* q(KT_e)^2}{h^3}\exp\left(-\frac{E_c-E_{Fn}}{KT_e}\right)\cdot\left[\exp\left(-\frac{E_1}{KT_e}\right)-\exp\left(-\frac{E_2}{KT_e}\right)\right] \qquad (2)$$

where, Q(t) is the trapped charge density per unit area in oxide, η is a fitting parameter after considering the tunneling effect and the probability for an electron from the Si substrate deep to the interface without inelastic collision.

Along with the increase of trapped charge in the gate oxide, the energy band of Si in region *B* will be raised, so the trapping probability for hot-electron will be decreased. The shift of E_2 (see Fig.3) can be written as :

$$\Delta E_2(t) = -\frac{q}{C_i}\left(\frac{1}{T_{ox}}\int_0^{T_{ox}} x\rho(x,t)dx\right) = \xi Q(t) \qquad (3)$$

where $\rho(x,t)$ is the volume charge density of trapped charge, and ξ is a fitting parameter related to the distribution of trapped charge. In [13], the distribution of trapped charge in oxide is thought to be uniform for n^+-polySi. We use a fitting parameter to include non-uniform distribution case.

After considering the change of energy band eq. (2) becomes :

$$\frac{dQ(t)}{dt} = -\eta\frac{4\pi m^* q(KT_e)^2}{h^3}\exp\left(-\frac{E_c - E_{Fn}}{KT_e}\right) \cdot\left\{\exp\left(-\frac{E_1}{KT_e}\right) - \exp\left(-\frac{E_2 - \Delta E_2(t)}{KT_e}\right)\right\} \qquad (4)$$

Solving eq.(4), we can get the following formula for Q(t) :

$$Q(t) = -\beta\left(1 - e^{-\alpha t}\right) \qquad (5)$$

where,

$$\begin{cases} \alpha = \eta\xi\dfrac{4\pi q m^* KT_e}{h^3}\exp\left(-\dfrac{E_c - E_{Fn}}{KT_e}\right)\exp\left(-\dfrac{E_2}{KT_e}\right) \\ \beta = \dfrac{KT_e}{\xi}\left(1 - \exp\left(-\dfrac{E_1 - E_2}{KT_e}\right)\right) \end{cases} \qquad (6)$$

The trapped electron raise the energy band level near the drain, this result in the increase of MOSFET's threshold voltage as well as some reliability problem. The threshold voltage of nMOSFET's in linear region is equal to the gate voltage that makes Si surface of region B strong inversion. So, the shift of nMOSFET's threshold voltage can be calculated by :

$$\Delta V_T(t) = -\frac{\xi Q(t)}{q} = \gamma\left(1 - e^{-\alpha t}\right) \qquad (7)$$

where,

$$\gamma = \frac{KT_e}{q}\left(1 - \exp\left(-\frac{E_1 - E_2}{KT_e}\right)\right) \qquad (8)$$

3. COMPARISION WITH EXPERIMENT DATA

The comparision between the calculated results with eq.(7) and experiment data is shown in Fig.4. In eq.(5), it predicts that the trapped electron in oxide will trend towards saturation while increasing the stress time.

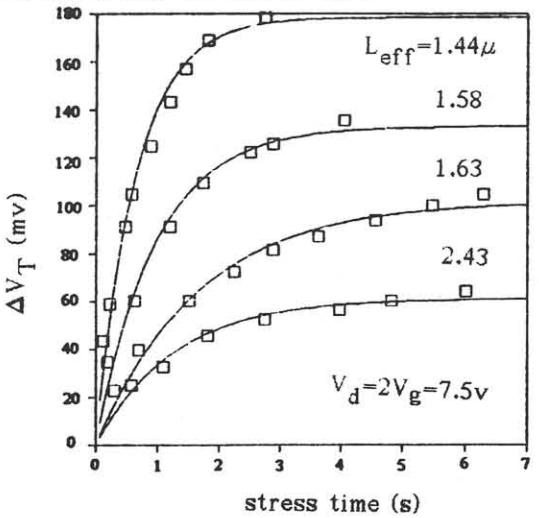

Fig.4 The relationship between ΔV_T and stress time t.

□□□ experiment data from [6]

—— calculated results

The saturation trend is caused by the negative feedback effect of trapped charge, that is, increasing the trapped charge will decrease the trapping probability of electron. The good agreement between the calculated results and experiment data confirmed that the threshold voltage degradation for nMOSFET's is mainly caused by trapped-electron in the gate oxide region, and this degradation can trend towards saturation.

4. DISCUSSION

The hot hole has little influence on nMOSFET's parameters degradation at general applied

bias condition. Because the hole temperature is much smaller than the electron temperature, as well as the Si-SiO_2 interface barrier for hole is much higher than that for electron. So, the emission probabilty of hole is much smaller than that of electron. Additionally, hole mobility in oxide is smaller than electron, hot holes mainly locate at Si-SiO_2 interface and are easy to be recombinated by injected hot electron.

Hot-electron-induced interface trap effect is unimportant compared with trapped electron effect on device parameters degradation. In [9], it is shown that hot-electron-induced interface trap is mainly located upon drain region, and the maximum measured interface trap in the channel region is $10^{11}cm^{-2}$. If oxide thickness is 150 A, threshold voltage degradation induced by interface trap is ~20mV, which is ~1/10 compared with that induced by trapped electron.

In eq.(7), E_1 and E_2 are functions of channel length and bias. So, the saturation ΔV_T is determined by stress condition and device structure. The shorter the channel length is, the higher the electron temperature is, and so the higher the saturation ΔV_T is. Moreover, saturation ΔV_T increases along with the increase of E_2-E_1.It is the same as experiment data.

5. CONCLUSION

A new threshold voltage degradation model is derived, in which, the nagative feedback of trapped electron to electron trapping has been included. The good agreement between new model and experimental data comfirmed the mechanism that nMOSFET's degradation is mainly caused by trapped electron in oxide region. The new model can indicate the saturation trend in the nMOSFET's degradation.

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