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Anomalous Band-to-Band Tunneling Current in n-ch MOSFETs

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An anomalous band-to-band tunneling current characteristic, that is a peaked structure in I_d-V_{sub} curve, was observed in n-ch MOSFETs. The detailed analysis clarified that it is characterized by band-to-band tunneling, hole trapping, and surface-breakdown. The peak-to-valley ratio for the I_d-V_{sub} curve decreased with gate oxide thinning and was not observed in MOSFETs with very thin gate oxides, T_{ox} = 4 nm. It has been demonstrated that the lateral electric field at the gate-drain overlap region strongly affects the band-to-band tunneling current and related phenomena.

1. Introduction

In scaled MOSFETs, band-to-band tunneling current causes fatal problems, such as drain leakage current or device degradation. However, it has only been so far discussed in a very simplified fashion from the viewpoint of one dimensional tunneling [1]-[5].

In this paper, anomalous behavior of band-to-band tunneling current observed in n-ch MOSFETs is reported for the first time. It is emphasized that the lateral electric field plays an important role in this anomalous band-to-band tunneling characteristic.

2. Experimental Results and Discussion

In this study, conventional n^+ polysilicon gate n-ch MOSFETs were used. Gate oxide thicknesses, T_{ox}, ranged from 4 to 34 nm, though 25 nm T_{ox} was used in many experiments. Channel length, L, was 5 μm. The surface impurity concentration of the p-type substrate was 1×10^{16} cm^{-3} and source/drain junction depth was 0.2 μm. The measurements were carried out with source-open and drain-grounded conditions, as shown in Fig.1.

Figure 2 shows the drain current measured by sweeping the substrate bias, V_{sub}, from 0 to -10 V for various gate biases at fixed V_d = 0 V in the band-to-band tunneling current regime. It is quite anomalous, in that the I_d-V_{sub} curve has a peaked structure and that the peak-to-valley ratio increases with $|V_g|$. By reducing oxide thickness in a fixed vertical electric field at the gate-drain overlap region, the peaked structure becomes indistinct, and then disappears in the MOSFET with T_{ox} = 4 nm, as shown in Fig.3.

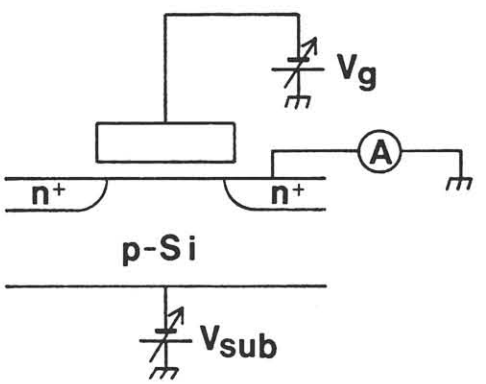

Fig.1 Schematic cross section of the MOSFET.

This anomalous I_d-V_{sub} curve seems to be associated with the relatively high lateral electric field at the gate-drain overlap region, because the drain-gate bias, that is the vertical electric field, is fixed during V_{sub} sweeping. Only drain-substrate bias is increased, as shown in Figs.2 and 3. On the other hand, the

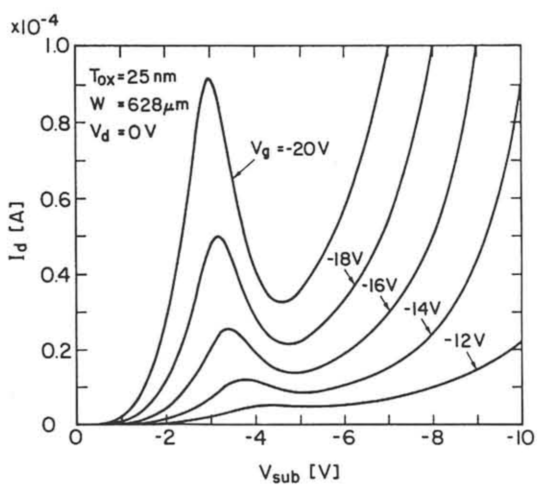

Fig.2 Typical I_d-V_{sub} characteristics. The I_d-V_{sub} curve for each V_g was measured by sweeping V_{sub} from 0 to -10 V and at fixed V_d = 0 V.

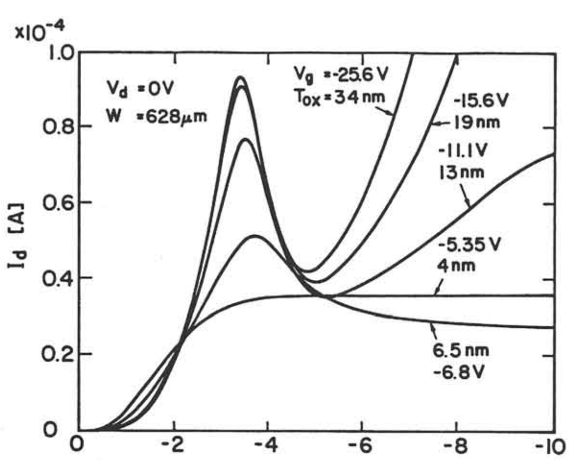

Fig.3 I_d-V_{sub} characteristics for various gate oxide thicknesses. Gate bias values are -25.6, -15.6, -11.1, -6.8, -5.35 V for T_{ox} = 34, 19, 13, 6.5, 4 nm, respectively.

I_d-V_{sub} curve in the second V_{sub} sweeping did not coincide with the initial one, but it was recovered by applying a positive bias to the gate, i.e. V_g = 20.3 V for 30 sec, as shown in Fig.4. These results strongly suggest that holes are trapped in the gate oxide during V_{sub} sweeping and that the vertical electric field at the gate-drain overlap region is reduced.

To quantitatively characterize this hole trapping behavior, the gate bias dependence of the band-to-band tunneling current was measured after stressing. In Fig.5, I_d-V_g

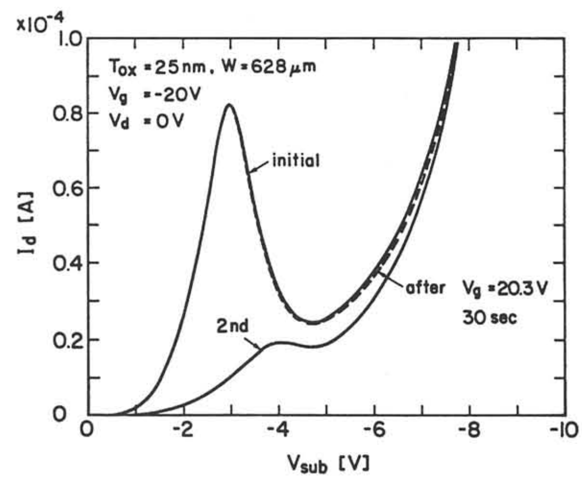

Fig.4 I_d-V_{sub} characteristic at initial and 2nd V_{sub} sweeping. The dashed line curve indicates I-V characteristics after being biased at V_g = 20.3 V for 30 sec.

curves are shown at V_{sub} = -2 V, after stressing at V_g = -20 V and V_{sub} values for 0.2 sec. These stress conditions are indicated by the characteristics "a" to "j". The drain current values at each stress condition are shown in the inset in Fig.5. The turn-on gate bias in the band-to-band tunneling current moves to the right (large $|V_g|$) with stressing conditions from "d" to "j", that is V_{sub} = -3 to -9 V. This voltage shift can be reasonably explained by the mechanism that some holes, left at the interface by the band-to-band tunneling, are accelerated by the lateral electric field, and that some of them are injected into the gate oxide and trapped there [6]-[8]. This leads to reduction in the band-to-band tunneling current.

The gate current was measured as a function of the substrate bias for T_{ox} = 15 nm to directly investigate the hole injection mechanism into the gate oxide. The applied gate and drain biases were -12.7 and 0 V, respectively. As shown in Fig.6, the gate current decreases and successively increases with $|V_{sub}|$. Taking into consideration that the vertical electric field at the channel region is relatively high at V_{sub} = 0 V and decreases with $|V_{sub}|$ and that the lateral electric field increases with $|V_{sub}|$, the F-N (Fowler Nordheim) tunneling current from the gate to the substrate and the injected hole current are considered to be dominant at $|V_{sub}|$ < 2 V and > 3 V, respectively. The injected hole current, that is the gate current

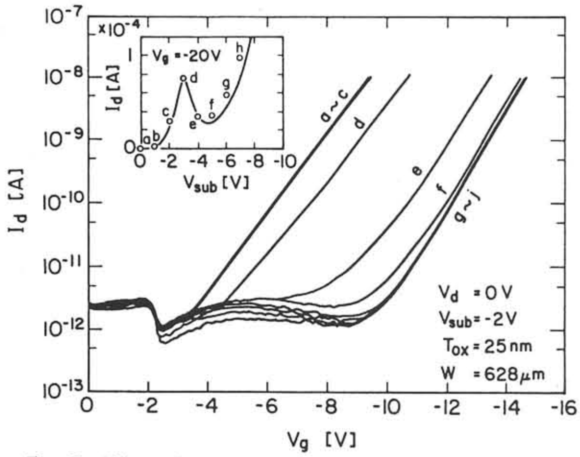

Fig.5 I_d-V_g characteristic for V_{sub} = -2 V after 0.2 sec stressing at V_{sub} and V_g = -20 V.

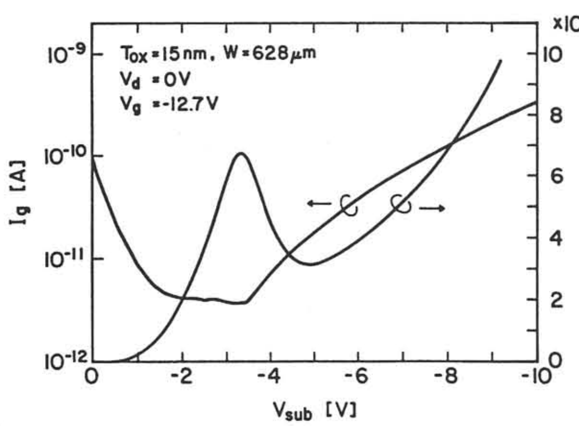

Fig.6 I_g-V_{sub} characteristic for T_{ox} = 15 nm at V_g = -12.7 V.

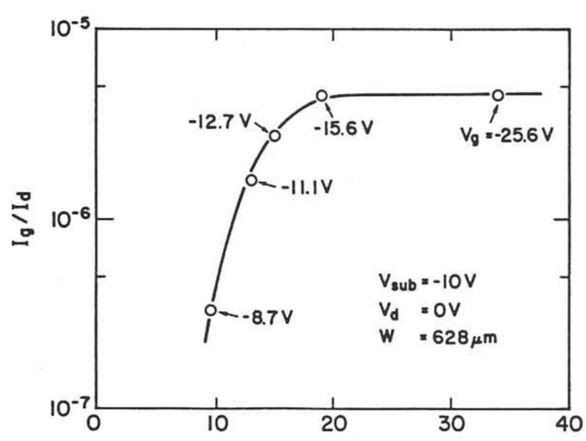

Fig.7 T_{ox} dependence of the I_g/I_d ratio at V_{sub} = -10 V. The gate bias values are -25.6, -15.6, -12.7, -11.1, -8.7 V for T_{ox} = 34, 19, 15, 13, 9.5, respectively.

at V_{sub} = -10 V, was measured in MOSFETs with various gate oxide thicknesses. As shown in Fig.7, this hole injection efficiency I_g/I_d is a strong function of the gate oxide thickness, when both the vertical electric field at the gate-drain overlap region and the drain-substrate bias are kept constant. This fact can explain the decrease in the peak-to-valley ratio in thin gate oxide MOSFETs as shown in Fig.3.

Figure 8 shows maximum lateral electric field E_x at the Si-SiO_2 interface in the gate-drain overlap region, which was calculated by a 2-dimensional device simulator, MOS2C [9]. When T_{ox} = 25 nm, E_x is larger than 1 MV/cm at $|V_{sub}|$ > 6 V. Thus, the holes created by the band-to-band tunneling at the gate-drain overlap region can become hot and can then be injected into the gate oxide. Moreover, the surface-breakdown will occur in this high lateral electric field regime. On the other hand, E_x in the 5 nm case is much smaller than that in the 25 nm case. Thus, the holes will not become hot. Therefore, the difference in the lateral electric field reasonably explains the fact that the hole injection rate decreases with the gate oxide thinning as shown in Fig.7 and that no anomalous I_d-V_{sub} curve was observed in the MOSFET with T_{ox} = 4 nm as shown in Fig.3.

The difference in the lateral electric field, between T_{ox} = 25 and 5 nm, is due to the 2-dimensional effect of the potential distribution at the gate-drain overlap region. In Fig.9, the contour plots for the potential distribution at V_{sub} = -5 V are shown. When T_{ox} = 25 nm, the channel region is strongly accumulated and the field induced junction is formed over the n^+ region. Thus, the drain-substrate bias is applied between n^+ and accumulated region. Then, the lateral electric field will locally become high. On the other hand, as it is depleted when T_{ox} = 5 nm, the drain-substrate bias is applied over a relatively wide depletion region. This change in the potential distribution is attributed to the voltage difference between the gate and substrate, i.e. 0 V and -15 V for T_{ox} = 5 and 25 nm, respectively.

3. Conclusion

An anomalous I_d-V_{sub} curve has been observed in the band-to-band tunneling regime. It has been clarified that it is caused by hole trapping and subsequent surface-breakdown. Moreover, it has been demonstrated that, not only the vertical electric field, but also the lateral electric field at the gate-drain overlap region should be essentially important to characterize the band-to-band tunneling and the related phenomena.

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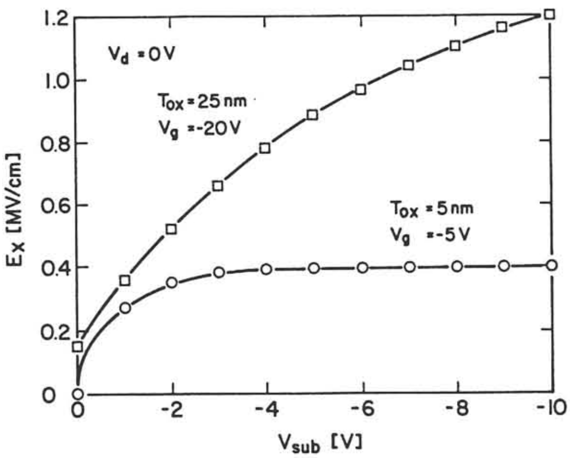
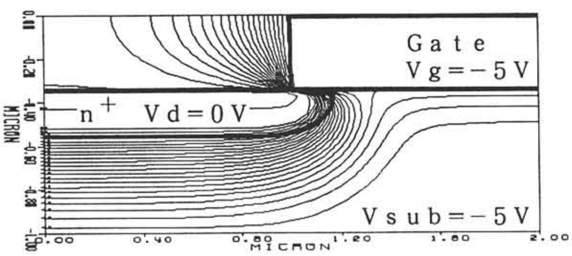
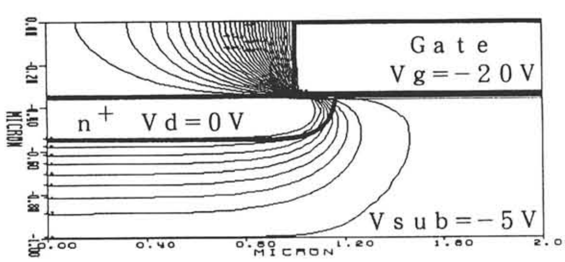


Fig.8 Calculated lateral electric field E_x for T_{ox} = 25 and 5 nm by 2-dimensional device simulator. V_g = -20 and -5 V for T_{ox} = 25 and 5 nm, respectively.



(a) T_{ox} = 5 nm



(b) T_{ox} = 25 nm

Fig.9 Potential distribution contour plot at V_{sub} = -5 V. (a) When T_{ox} = 5 nm. (b) When T_{ox} = 25 nm. V_g values are -5 and -20 V for T_{ox} = 5 and 25 nm, respectively.