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Comparative Study of HC-Degradation of NMOS and PMOS Devices with n^+ and p^+ Gate: Experiments and Simulation

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A comparative study of hot-carrier degraded NMOS and PMOS devices with either n^+ or p^+ gates is presented. Utilizing our new simulation tool, we have performed a very detailed analysis of the experimental results. To simulate hot-carrier degradation we have extended MINIMOS in a way which allows to directly monitor the build up of charge and interface states during the DC stress experiment. The direct comparison of experimental and simulation results provides new insights in the physics of hot-carrier degradation of advanced submicron CMOS devices with n^+ and p^+ gate material.

1. INTRODUCTION

The increasing level of miniaturization puts severe constraints upon the performance of MOSFET devices. Utilizing dual work-function techniques permits that NMOS and PMOS devices in one CMOS technology are both surface channel devices, which have an improved short channel behavior[1]. However, on the expense of a higher process complexity and cost. Another major concern in device design is long term stability. In this presentation we will present a comparative study of hot-carrier degraded NMOS and PMOS devices with either n^+ or p^+ gates. We give a very detailed analysis of the experimental results[2] utilizing our new simulation tool[3] that allows to directly monitor the build up of charge and interface states during the DC stress experiment.

2. EXPERIMENT

A twin-well CMOS process with splitted well drive-in, LOCOS isolation and 16nm gate oxide was used to realize n^+/p^+ gate CMOS devices with channel length down to 0.4um. Except for the gate definition sequence, the processing was identical for both types of devices. For the n^+ gate devices conventional phosphorous doped poly silicon was used. The p^+ gate version consisted of boron doped $TaSi_2$/poly silicon bilayers (polycide). The silicide films were prepared by cosputtering Ta and Si from separate targets. A LTO-cap was used to mask the gates against counterdoping from S/D implants. Conventional BPSG reflow, single level metalization and a forming gas anneal completed the process. Hot-carrier degradation experiments were performed by means of conventional DC stressing. The hot-carrier stress of the NMOS device was performed at maximum substrate current, whereas the PMOS was stressed at maximum gate current. The devices were characterized in the linear mode at V_D=0.1V. Charge pumping measurements were performed to evaluate the number of interface traps prior and after stress.

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3. SIMULATION

To simulate the DC stress experiment we have extended MINIMOS to solve the complete set of semiconductor equations in the oxide region of a MOSFET. We therefore obtain the spatial distribution of minority and majority carriers that were injected into the oxide through the Si/SiO_2 interface. The oxide current densities obtained in such a way are then taken as input for a generalized trap rate equation that includes the formation of positive and negative oxide charges, creation of acceptor and donor like interface states, and trap generation by high energetic particles in the oxide. During the temporal development of the trap scenario we fully account of the feed back of oxide charges and interface states onto the fields and carrier distributions in the active device area.

4. RESULTS

In Fig 1. we show the measured and calculated life time data for the NMOS devices. Sample A is the surface channel device and sample B a buried channel type with a shallow channel junction. The life time of the surface channel device is significantly shorter than that of the buried channel device. In Fig. 2 we show the self consistently calculated time development of the maximum interface charge during the DC stress experiment at maximum substrate current. Type A is the surface channel device, B and D are buried channel devices with shallow and deep channel junctions, respectively. We find that for larger stress times the amount of effective interface charge correlates with depth of the channel junction and is consequently largest for the surface channel device. Charge-pumping measurements in Fig. 3 show that the total number of interface states that are created during the stress experiment is comparable for the surface channel device A and the buried channel device B, but less for device D which has a deep channel junction. The reduced degradation in the buried channel device is the consequence of a lower interface minority carrier density which pulls the quasi Fermi level towards mid gap and henceforth reduces the effective interface charge. The different slope observed in the

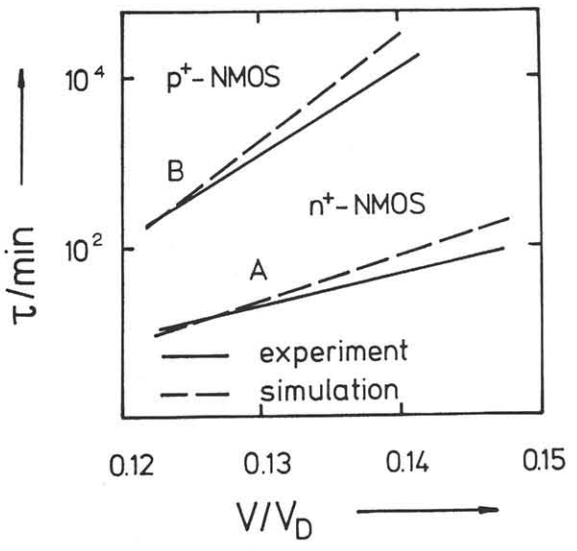

Fig.1 Comparison of life time of p^+ and n^+ NMOS devices with effective channel length L_{eff}=0.8um. Solid line - experiment, dashed line - simulation. A is a surface channel LDD and B a buried channel device with As compensation doping of 1.4 x $10^{12}cm^2$, 100keV and identical S/D complex as A.

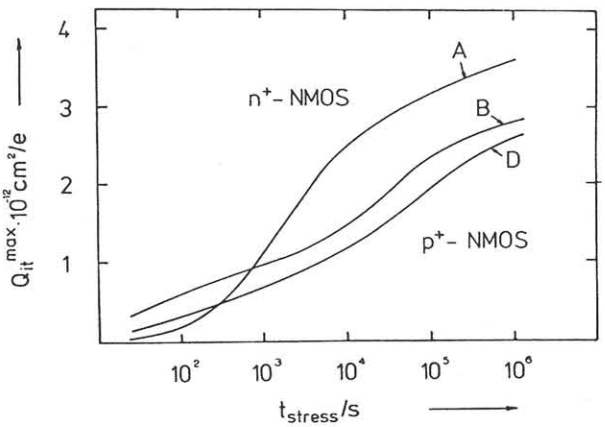

Fig.2 Time evolution of maximum interface state charge during stress experiment. A and B are the devices specified in Fig.1. The device D is a buried channel device with 1.8 x $10^{12}cm^2$, 160keV As compensation implant.

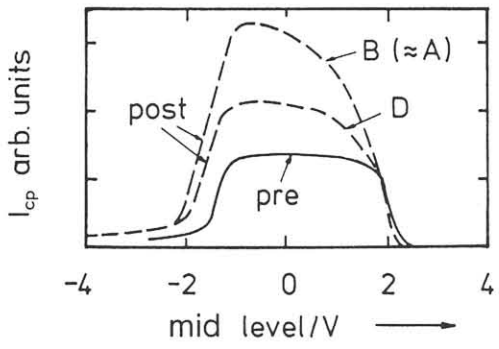

Fig.3 Charge-pumping current prior and after stress for devices specified in Fig.'s 1 and 2.

experimental data can only be obtained if we increase the hole trap density for the p^+-NMOS device by a factor of two. This might be related to the different process required for the formation of the p^+-polycide gate[2].

In Fig. 4 we show the change of drain current due to stress induced oxide charge for the PMOS devices in the linear regime. The buried channel device is more effected than the surface channel device. Its life time is reduced by approximately 80% compared to the surface channel device. In Fig.5 we show the calculated change in drain current for the PMOS device. We find the same trends as observed in the experiments. If we include the mobility degradation due to oxide charges, which always leads to a decrease of current,

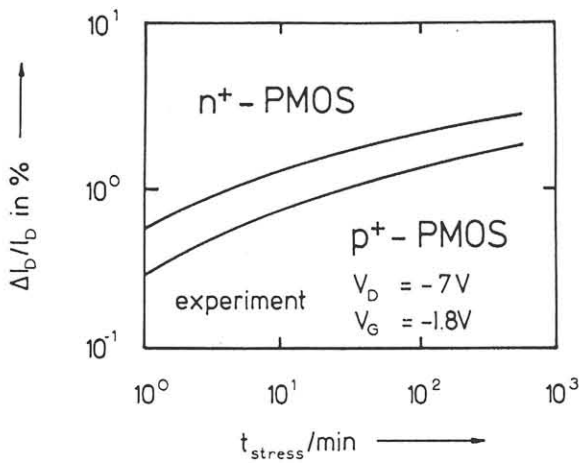

Fig.4 Time evolution of drain current during stress: experimental data.

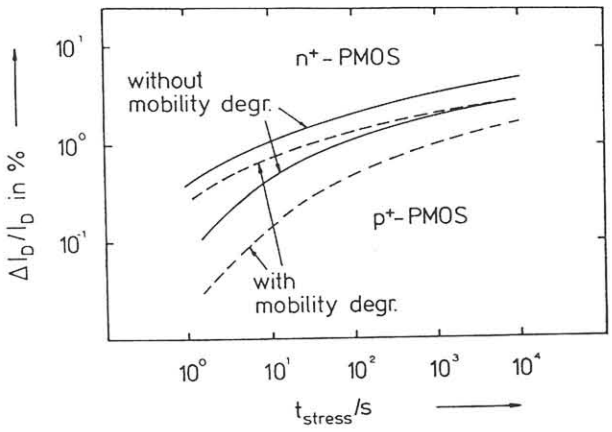

Fig.5 Time evolution of drain current during hot-carrier stress: simulated data. Solid lines - no mobility degradation, dashed lines - maximum mobility degradation.

degradation is slowed further down counteracting the increase of current due to the potential effect. In Fig. 6 we show the measured substrate and gate current for the considered PMOS devices. We see that the order of substrate and gate current is reversed. This behavior is explained by the different temperature distribution along the Si/SiO_2 interface for minority and majority carriers in the surface channel and buried channel PMOS, respectively, as shown in Fig.'s 7 and 8. The holes have a considerable higher temperature in the former than in the latter which correlates with the substrate current. For the

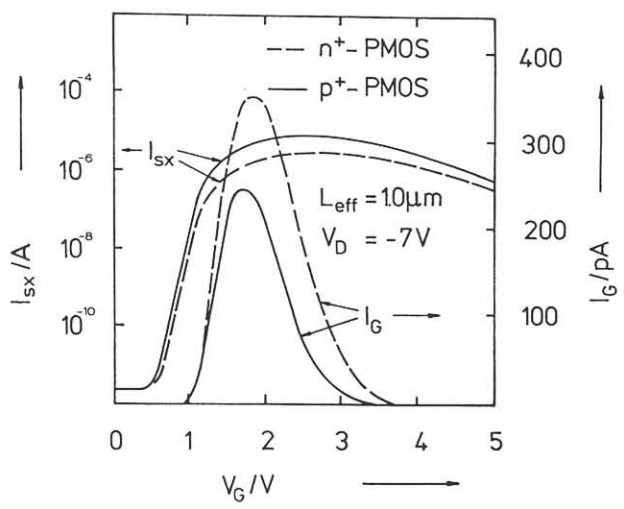

Fig.6 Substrate and gate currents for n^+ and p^+ gate PMOS: experimental data.

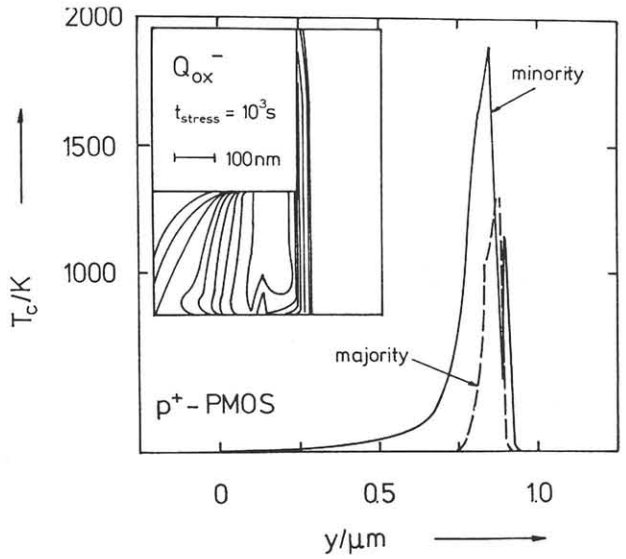

Fig.7 Minority and majority carrier temperatures along the interface for p+ PMOS. The insert shows the trap distribution at $t=10^3$sec.

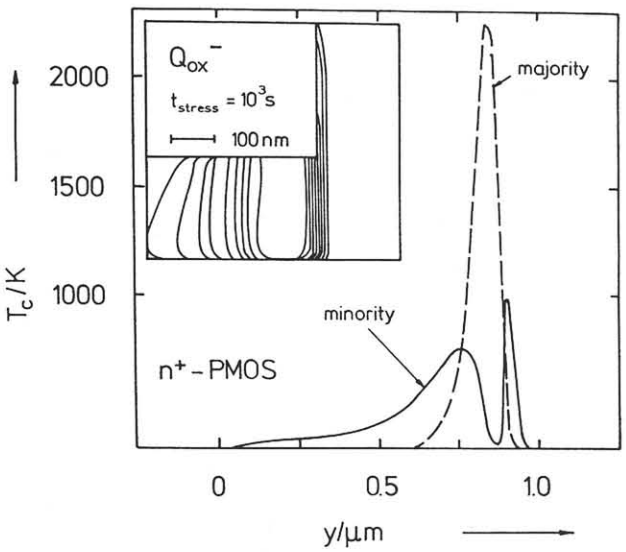

Fig.8 Minority and majority carrier temperatures along the interface for n^+ PMOS. The insert shows the trap distribution at 10^3sec.

electrons we find the opposite result which correlates with the gate current. The physical reason for this behavior is that minority carriers are heated up in the lateral electric field to generate majority carriers which gives the substrate current. The majority carriers are heated up in the transverse electric field and are injected into the gate oxide to give the gate current. Because the position of maximal impact ionization is deeper in the buried channel device the electrons can pick up more energy in the transverse field and this gives a higher gate current in the n^+gate PMOS. We also show as an insert in Fig.'s 7 and 8 the distribution of negative oxide charge after 10^3s stress time. There is a characteristic difference in the p^+ and n^+ PMOS. Due to the enhanced injection of holes, negative charge near the interface is compensated. That moves the center of charge into the gate oxide. As a result it less effects the drain current.

5. CONCLUSION

We have presented a comparative study of hot-carrier degradation of NMOS and PMOS devices with n+ and p+ gate material. If the device is sized only with respect to its hot-carrier stability we find the burried channel NMOS and the surface channel PMOS to be the best alternative. This would imply a CMOS technology with p+ gate material. There are, however, other device parameters to be considered, e.g. off-current or subthreshold slope, to obtain optimal performance. The choice of the work-function combined with suitable drain engineering will therfore provide the device engineer with a large variety of options to find the best device.

6. REFERENCES

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