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Band-to-Band Tunneling Current as a Probe for the Hot-Carrier Effects

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Abstract

The band-to-band tunneling (BBT) current characteristics are studied as a probe for the oxide trap charge generation due to the hot carrier effects in Nch MOSFETs. It is shown that there is a considerable amount of oxide trap charge generation in the gate-to-drain overlap region and it shows a logarithmic time dependence ($\propto \ln t$), which is different from that of the interface states generation which has a power-law time dependence ($\propto t^{n}$ (n<1)).

1. Introduction

It is well known that the hot carrier induced degradation in MOS devices is caused by the interface state generation and the electron or hole trapping in the oxide[1~2]. The interface state generation can be best measured by means of the charge pumping technique[3], and has been intensively studied in the last few years, as the main cause of degradation in Nch MOSFETs. On the contrary, the charge in the oxide traps (electron or hole traps in bulk oxide) cannot be measured directly and it is difficult to distinguish oxide trap charge from the charge of the occupied interface states. Recently a new type of leakage current between drain and substrate in thin gate oxide MOSFETs has been reported and it was shown to be caused by band-to-band tunneling (BBT) in the deep depletion layer formed beneath the gate-to-drain overlap region[4]. And it turned out to be sensitive to the hot carrier injection into the oxide[5].

In this paper, it is reported that the BBT current characteristics can be used as a good probe for the oxide trap charge generated by the hot carrier effects. And it will be shown that oxide trap charge generation has a different behavior from that of the interface state generation.

2. Band-to-band tunneling current characteristics and trapped charge in the oxide

Fig.1(a) illustrates the oxide trap charge and the band-to-band tunneling region in a MOSFET, and Fig.1(b) shows the band diagram of the Si/SiO_2 interface in the band-to-band tunneling region. The tunneling characteristics are determined only by the band bending and must be a function of (Vd–Vg). When electrons or holes are trapped in the oxide, the band-bending is varied corresponding to the surface potential shift due to the trapped charge, leading to the shift of the BBT characteristics as shown in Fig.2. The shift can be interpreted as the surface potential shift in the BBT-region, and is directly related to the trapped charge density as the following expression,

$$\Delta V_{bend} = \frac{q_0}{\varepsilon_0 \varepsilon_{ox}} \int x N_{trap}(x) dx$$

where $N_{trap}(x)$ is the trapped charge density [cm^{-3}] at a position x in the oxide, the integration is through the oxide thickness. The accuracy in the measurement of the surface potential shift is about 10mV,which corresponds to 2.70×10^{10} cm^{-2} of the oxide trap density when $N_{trap}(x)$ is uniform in the oxide, or 1.35×10^{10} cm^{-2} when $N_{trap}(x)$ is localized at the Si/SiO_2 interface, in the case that the oxide thickness is 160 Å.

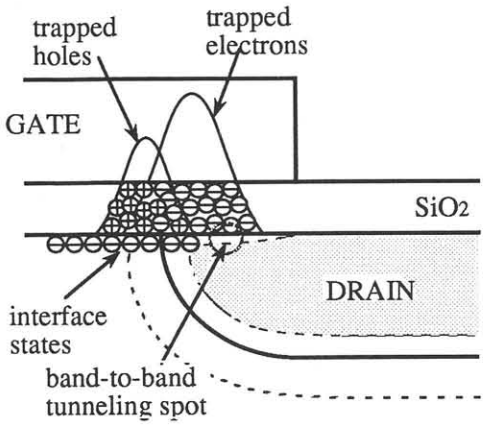

Fig.1(a) Electron- and hole-traps and the band-to-band tunneling spot region

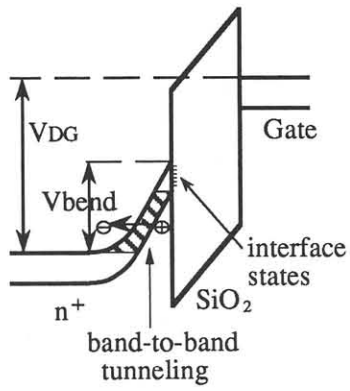

Fig.1(b) Band diagram at the Si/SiO_2 interface (Gate/Drain overlap region)

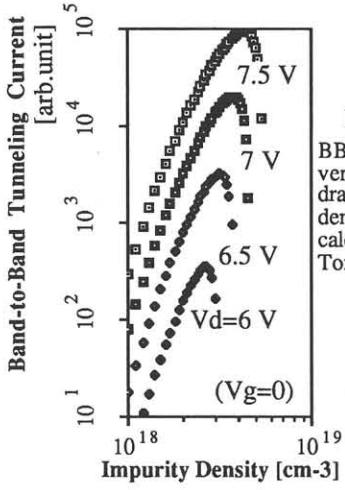

Fig.3 BBT current versus drain impurity density [6] calculated for Tox=160A

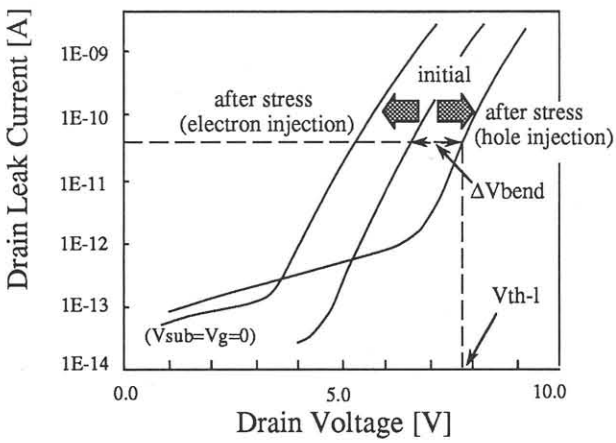

Fig.2 Band-to-band tunneling current characteristics before and after hot carrier stress

There are following prominent features in this method.

(1) It detects only the effect of the trapped charge in the oxide and cannot be affected by the interface states, because the interface states are much higher than the Fermi level so that the all interface states are empty and have no charge when the BBT current flows(Fig.1(b)), assuming that the generated interface states are dominantly acceptor-like.

(2) It detects the surface potential shift at a specific point in the gate-to-drain overlapped region (not the information averaged through a broad region). It was pointed out[6] that the BBT current has a strong dependence on the doping density and it flows only at the doping density of about 10^{18} cm^{-3} as shown in Fig.3. Considering the doping density profile along the gate-to-drain overlap region, the BBT is highly localized in a small region of the size of about a few hundred Å where the doping density crosses the values of about 10^{18} cm^{-3}. Interestingly, the current peak position shows a small shift as Vd (and the total current) is increased. This is consistent with the fact that the BBT current characteristics-shift (along Vd-axis) is observed larger at a small current value and smaller at a large current value as shown in Fig.2, because the trap charge has a profile as shown in Fig.1(a) and the BBT spot tends to shift toward the drain as the current becomes larger. Although the current peak position shows a small shift as Vd is increased, the BBT current characteristics shift at a specific current value corresponds to the surface potential shift at a specific point in the gate-to-drain overlap region.

3. Experiments and results

The samples used are conventional poly-Si gate Nch MOSFETs of the single drain structure (L=0.9 μm, W=16.0 μm) . The gate oxide was formed by dry oxidation at 950℃ and the thickness is 160 Å. The source/drain region was doped with As.

The surface potential shift at the BBT region was measured as the shift of V_{th-l}, which is defined as the drain voltage where the BBT current exceeds the value of 5×10^{-11} [A], when the gate voltage is kept constant and the substrate is biased to 0 [V]. During measurements, the BBT current was kept below 1×10^{-10} [A], to prevent hot-carrier injection due to the BBT current stress itself. Fig.4(a),(b),and (c) shows the stress time dependence of Vth and Vth-l for stress conditions:

(a) Vd=7.8 [V] , Vg=3.9 [V] (both electrons and holes are injected : Isubmax condition)

(b)Vd=7.1[V],Vg=7.1[V] (electrons are mainly injected)
(c) Id =2 [μA] , Vg=0 [V] (holes are mainly injected)
,respectively. The values of Vth-l are plotted for two values of Vg(0 and -1[V]) in the BBT current measurement. The fact that the two Vth-l values are separated by about 1 [V] assures that the current is due to the BBT in the band-bending between gate and drain.

It is noticeable that a considerable amount of electron traps are generated in the region over the drain. In Fig.4(a) and (b),the surface potential of the region where band-to-band tunneling takes place shifts as large as about 1 V, even when there is still only a few mV shift of Vth. Such a large amount of electron trap charge causes a strong reduction in the carrier density in the surface of the drain, which could explain a large conductance reduction specially in the early stage of degradation.

Fig.4(a) clearly shows the difference between the time dependences of V_{th} and $V_{th\text{-}l}$. While V_{th} varies as a power law of time t ($\propto t^n$), $V_{th\text{-}l}$ shift shows a logarithmic dependence on time ($\propto$ ln t). V_{th} shift is considered to be due to the interface state generation and it varies as t^n. On the other hand, $V_{th\text{-}l}$ shift represents the oxide charge trapping and observed to vary as ln t. This logarithmic time dependence can be explained by the Verwey's model[7], which has been proposed to explain the walk-out phenomena of the drain breakdown voltage due to hole injection into the oxide. Verwey assumed a field dependent carrier injection rate, and supposed that the field is modified by injected charge in the oxide, thus leading to the ln t - dependence of the potential shift. This can be applied also to the case of electron injection, except that the sign of the shift is reversed. The observed difference of the time dependence suggests that the mechanism of the interface state generation is not directly related to the charge injection or the charge trapping in the oxide.

In the case of high-gate bias stress condition (the case (b)), $V_{th\text{-}l}$ shift shows the same logarithmic time dependence, corresponding to electron trapping in the oxide. V_{th} shift shows a power law dependence on time as in the Isubmax-case, suggesting that the interface state generation still is the main cause for the change. But the slope of the curve is smaller than the Isubmax-case, and the time dependence is closer to the logarithmic one,

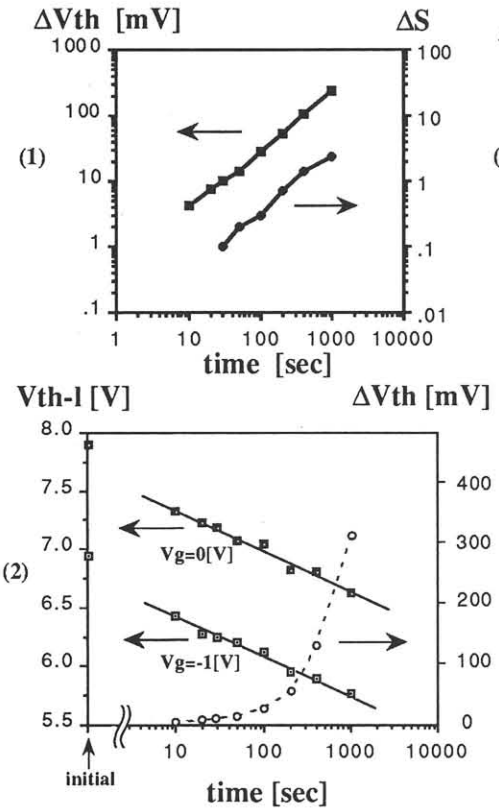

Fig.4(a) The stress time dependence of
(1) Vth-shift and subthreshold-swing (log-log plot), and
(2) Vth-l and Vth-shift (linear-log plot)
(stress: Vd=7.8 [V],Vg=3.9[V])

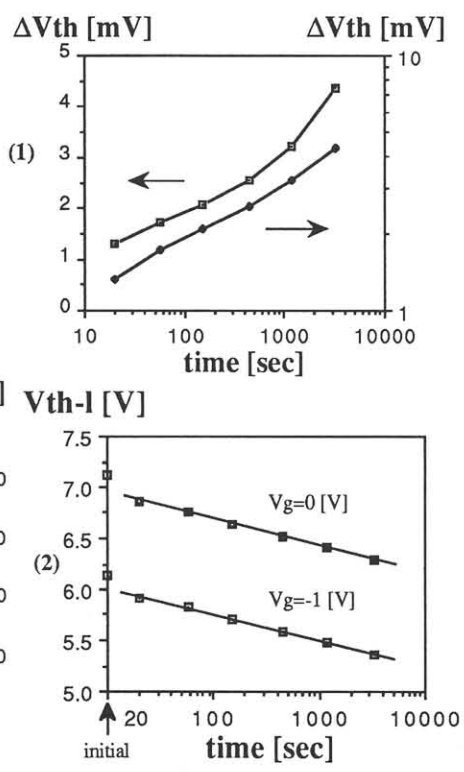

Fig.4(b) The stress time dependence of (1) Vth-shift (both in linear- and in log-plot), and
(2) Vth-l (in log-log plot)
(stress: Vd=7.1 [V],Vg=7.1[V])

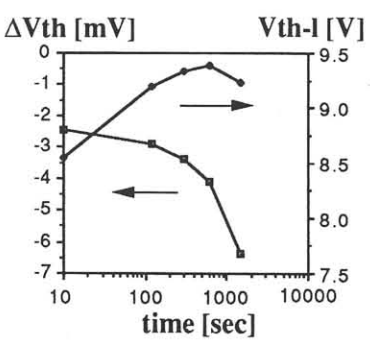

Fig.4(c) The stress time dependence of the Vth-shift and Vth-l (stress: Id=2[uA],Vg=0)

showing the dominance of the contribution from trapped charge in the oxide at least in the early stage of degradation.

In the case of low gate bias stresses ($V_g \sim V_{th}$), it is expected that holes are mainly injected[2] in the oxide leading to the positive V_{th-1} shift. However, the observed V_{th-1} shows a negligible or a small negative shift, instead of a positive shift. This can be understood by considering the difference between the space distribution of electron injection and hole injection. As shown in Fig.1(a), the distribution of the hole injection has a peak closer to the channel, while the electron injection takes place in the drain side of the junction. Therefore even at low gate biases where holes are injected into the oxide above the channel region, electron trapping appears to be dominant in the BBT region. Hole injection is observed when the device is stressed with off-state bias conditions (Vg<=0). In Fig.4 (c), V_{th-1} shift shows hole injection in the BBT region, which is saturated possibly because of the trap center filling, and then electron trapping appears after that.

It must be noted that there is a non-idealistic feature in the BBT current characteristics observed experimentally. Fig.5 shows the observed Idrain-Vg curves for different values of Vd (Vsub=0). If the current is fully of tunneling-nature, it must be a function of only the difference of Vg and Vd, and therefore 1 V change of Vd should exactly correspond to 1 V parallel shift of the Idrain-Vg curve along the Vg-axis. But the observed Idrain-Vg curve shows that the BBT current seems to be diminished as Vd(and so the lateral electric field)

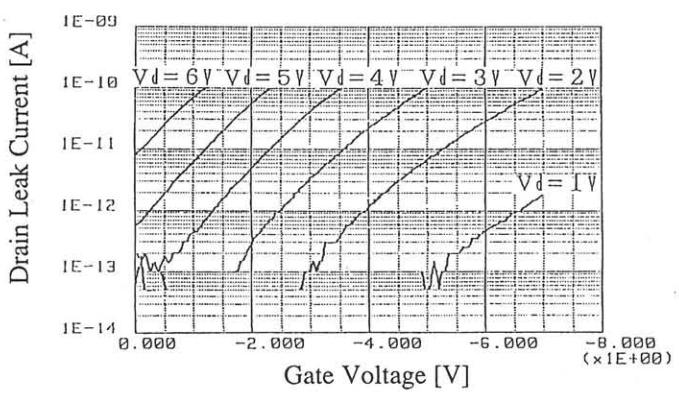

Fig.5 The band-to-band tunneling current characteristics for different bias conditions

becomes smaller. This non-idealistic behavior could possibly be related to the 2-dimensional effects as the followings, (i) The valence band becomes hole-rich and electron-deficient due to the extension of the hole-accumulated channel region toward the drain, (ii) The current becomes transport-limited rather than tunneling-limited (Noble et.al. pointed out the possibility that the generated minority carriers in the gate-to-drain overlap region could flow out via transport-limited process (diffusion) along the overlap region[8].).

In order to avoid such non-ideality, the measurements were performed by the condition that V_{th-1} is measured at large values of Vd (>5 [V]) with Vsub=0 and Vg kept at low values (0 or –1 [V]).

4. Summary

The BBT current characteristics were used as a probe for the trapped charge in the oxide, and a considerable amount of electron trapping and surface potential shift were observed in the gate-to-drain overlap region at the doping density of about 10^{18} cm^{-3} . The observed electron trapping in the oxide shows a logarithmic time dependence ($\propto$ ln t), which is distinct from that of the interface states which has a power-law time dependence ($\propto t^n$ (n<1)). This logarithmic dependence can be understood by the walk-out theory by Verwey.

References

1) C.Hu,S.Tam, F.-C.Hsu, T.Y.Chan, and K.W.Terrill ,IEEE Trans. Electron Devices, ED-32,375(1985)

2) T.Tsuchiya, T.Kobayashi, and S.Nakajima, IEEE Trans. Electron Devices, ED-34,386(1987)

3) P.Heremans et.al. IEEE Trans. Electron Devices, ED-35,2194(1988)

4) T.Y.Chan, J.Chen, and C.Hu, IEDM-87, 718(1987)

5) Duvvry, D.J.Redwine, and H.I.Stiegler, IEEE Electron Device Lett., EDL-9, 579(1988)

6) R.Shirota, T.Endoh, M.Momodimi, R.Nakayama, S.Inoue,R.Kirisawa,and F.Masuoka,IEDM88,27(1988)

7) J.F.Verwey, A.Heringa, R.de.Werdt, and W.V.D.Hofstad,Solid-State Electronics,20,689(1977)

8) W.P.Noble, S.H.Voldman, and A.Bryant, IEEE Trans. Electron Devices, ED-36, 720(1989)