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Robustness of LDD nMOS Transistors Subjected to Measurement of Drain Breakdown Voltage

Shian Aur and Amitava Chatterjee

Texas Instruments, Inc.
P.O. Box 655621, MS 369
Dallas, Tx. 75265, USA

We report a new measurement robustness concern observed in salicided LDD nMOS transistors which was traceable to a low-current snapback phenomenon. It is shown that this phenomenon is different from that described by the usual bipolar action models since the threshold current to snapback is about two to three orders of magnitude lower than the bipolar action model predicts. We speculate that this low-current snapback phenomenon is due to non-uniform (filamentary) current flow when the gate is grounded. We show that process parameters and the measurement technique can be modified to prevent this damage.

I. Introduction

Breakdown voltage of MOSFETs (BVdss) is an important parameter to monitor for submicrometer device. This is to insure reliability respect to punch through and avalanche-induced parasitic bipolar action. For long-channel transistors the I-V characteristics are typical of a junction reverse breakdown characteristic with the current flowing between the drain and the substrate contacts. As the channel length decreases, the grounded-gate nMOS breakdown characteristics exhibit a snapback phenomenon. In the current understanding[1-3] this negative differential resistance has been attributed to positive feedback caused by bipolar turn-on of the source-substrate junction. The usual snapback is initiated by electron-hole pairs generated in the drain depletion region. With the holes flowing to the p-type substrate the substrate potential is raised near the drain. If the channel length is short, i.e. the source is near the drain, then the source-substrate junction becomes forward biased resulting in electron injection from the source. Positive feedback is provided as this electron current causes more electron-hole pairs to be generated by impact ionization which, in turn, further raises the substrate potential. Thus, according to the bipolar turn-on models the threshold current for snapback to occur must be adequate to raise the substrate potential by about 0.6 V.

In this paper we report a new snapback phenomenon which occurs at a typical threshold current of about 100 nA and in some cases as low as 1 nA. The occurrence of this phenomenon at such low current levels precludes the usual explanation of snapback described above. More importantly, the presence of the low-current snapback phenomenon is related to robustness of nMOS transistors with respect to breakdown voltage measurements.

II. Failure mode and low-current snapback

The salicided LDD nMOSFETs used in our experiments all have width of 10 μm and the gate-oxide thickness is 20 nm. The process technology is described in reference[4]. The experimental set-up for the BVdss measurement is shown in Fig. 1. The transistor I-V curve is shown in Fig. 2 before and after the BVdss measurement. It is shown that the stress during BVdss measurement results in an anomalous increase in the leakage current. In the BVdss measurement no external resistor is used, i.e., $R_d = 0$ and the current compliance is set to 1 μA. Electrical characterization shows (Fig. 2 inset) this leakage to be

typically a resistive short between source and drain with a resistance between 100 kΩ and 10 MΩ. Subsequent analysis with infrared emission microscopy reveals filamentary conduction at the damage site. Thus the failure mode is similar to that during second breakdown caused by ESD stress[5].

We have traced this lack of robustness of the transistor to electrical overstress caused by equipment transient and found it to correlate with an anomalous snapback phenomenon occurring at extremely low currents. This is not the usual parasitic bipolar action since the current level is about two to three orders of magnitude less than the bipolar action model predicts. The experimental setup is the same as shown in Fig. 1 with $R_d \neq 0$ on 10 μm wide nMOS transistors of varying channel length and results are shown in Fig. 3. Drain current (I_d) is measured directly and drain voltage (V_d) is computed by subtracting $I_d R_d$ from the potential at the voltage source. Alternatively a current source could be used to measure the I_d-V_d characteristics. In either case R_d has to be connected to prevent sensitive devices from being damaged by transient currents. From the I_d-V_d results shown in Fig. 3, we observe the low-current snapback in the 0.8 μm and 1 μm channel length devices, but not in the devices with channel length of 2 μm and 0.7 μm. By measuring the source current I_s we determined that the 0.7 μm channel length device punches through ($I_d = I_s$) at a voltage lower than that required for avalanche breakdown. By adjusting the gate and substrate bias on the 0.7 μm length device, punch through can be suppressed and low-current snapback can be seen.

The observation that the low-current snapback phenomenon disappears if the channel lengths are either too short or too long suggests a combination of punch through and avalanche to be responsible. This particular feature of low-current snapback would be consistent with computer simulations done by Muller[6] et al. who found enhanced hole density at the surface near the source during impact ionization at the drain junction. However, to the best of our knowledge, there is no theory that can explain all the features of the low-current snapback that we have observed. We speculate that the current flow is not uniform when the gate is grounded and the Muller model is applicable only for the case when the channel is on and the current flow is uniform. For those devices exhibiting low-current snapback, a corresponding device failure is seen if no external resistor is used ($R_d = 0$) in BVdss testing, even with a current compliance as low as 100 nA on the HP4145 semiconductor parameter analyzer, whereas the rest of the devices remain undamaged even for a compliance limit set as high as 10 μA.

To further establish the correlation between robustness and the low-current snapback phenomenon we have performed the breakdown measurement with 1.0 μm channel length devices biased such that the low-current snapback is absent. As shown in Fig. 4 increasing the barrier for electrons at the source by negative gate bias eventually eliminates snapback at low currents. Similar effects are observed by varying the substrate bias.

III. Substrate resistance measurement

In order to demonstrate that the ohmic drop in the substrate is several orders of magnitude lower even if current spreading effects are taken into account we developed a new technique to estimate the substrate resistance seen from the drain end. We vary an external substrate resistor and observe the onset of bipolar turn-on from the clamping of the substrate current I_{sub} versus gate voltage V_{gs} curve[3]. The set-up is shown in the inset of Fig. 5 where the external substrate resistor is denoted by R_b. As shown in Fig. 5, the plot of I_{sub} versus V_{gs} for $R_b = 300$ kΩ has a flat region. This flat region occurs because forward biasing of the source-substrate junction causes any additional hole current to flow to the source contact. Let I^o_{sub} denote the value at which I_{sub} gets clamped, i.e., the flat portion of Fig. 5, and let R_{int} denote the unknown internal substrate resistance. Then

$$I^o_{sub} \times (R_{int} + R_b) = C \qquad (1)$$

where C is a constant roughly equal to 0.6 V corresponding to the forward bias at which the source-substrate junction is significantly turned on. From eq.(1)

$$1/I^{o}_{sub} = 1/C \times (R_{int} + R_b) \qquad (2)$$

Thus a plot of $1/I^{o}_{sub}$ versus R_b will show a straight line, as shown in Fig. 6, and the slope is $1/C$ and the intercept on the x-axis will give R_{int}. The internal substrate resistance obtained using this technique was about one kΩ. Thus, the low-current snapback phenomenon can not be be explained by the usual snapback mechanism. Indeed, despite using R_b = 300 kΩ the parasitic bipolar does not turn on until I_{sub} is about 2 μA (Fig. 5).

IV. Methods for robustness improvement

There are two ways to improve the robustness: to make the device more robust and to make the measurement more robust. For the device robustness, it is found that the p-well concentration is the most sensitive parameter to affect the device robustness with respect to BVdss measurement. The higher p-well dose will reduce the positive feedback for snapback as can be seen by comparing the I_d-V_d curves of three transistors shown in Fig. 7. BVdss measurements are subsequently performed using the HP4145 semiconductor parameter analyzer with R_d = 0 in the set-up shown in Fig. 1. We use the highest current compliance limit for which failure does not occur as a measure of robustness. The results, using this measure to compare the robustness of various transistors as shown in Table 1. Observe that the robustness is improved by increasing the p-well doping. This observation has been confirmed[7] by using the Krieger technique[8] to measure robustness.

For improving the measurement robustness, there are several choices. A resistor can be connected to the drain in series which will limit the equipment transient and prevent the device from being damaged. However, this may not be practical for some automated test equipment. Also since robustness is correlated with the low-current snapback phenomenon which can be controlled by gate and substrate bias. Thus the measurement robustness can be improved by appropriately biasing the transistor prior to the breakdown measurement as shown in Fig. 4. It is possible to find a test condition which will simultaneously eliminate low-current snapback and yield a breakdown voltage approximately equal to BVdss.

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Technology	W/L (μm)	P-Well Dose/cm^2	R_{sub} (Ohm)	BV_{dss} Robustness
A	10/1	1.4x10^{12}	4500	Ic < 10 nA
B	10/1	2.5x10^{12}	3500	10 nA < Ic < 100 nA
C	10/1	1.0x10^{13}	250	10 μA < Ic

Table 1 Process comparison of BVdss robustness with various p-well dose.

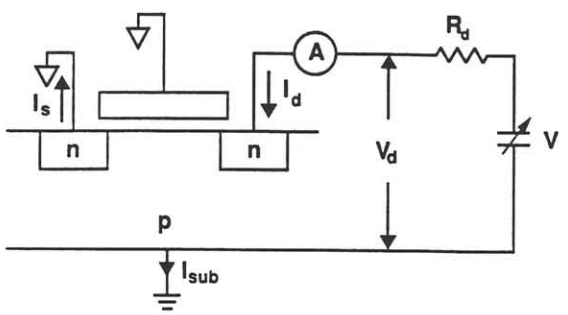

Fig. 1 Experimental set up for BVdss measurement, normally R_d=0.

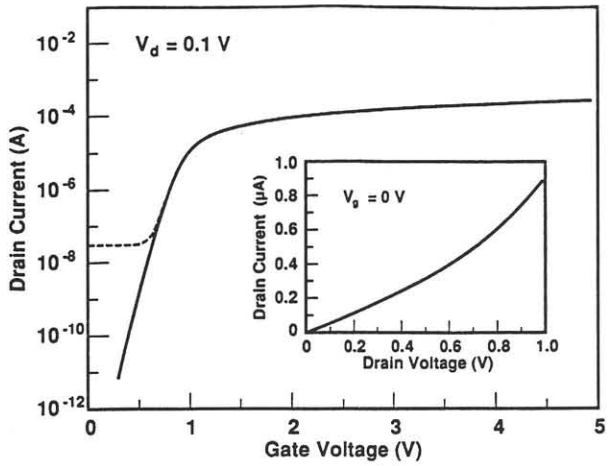

Fig. 2 Transistor transfer curve measured before (solid) and after (dashed) BVdss measurement. The leakage current after is a resistive short between source and drain as shown in the inset.

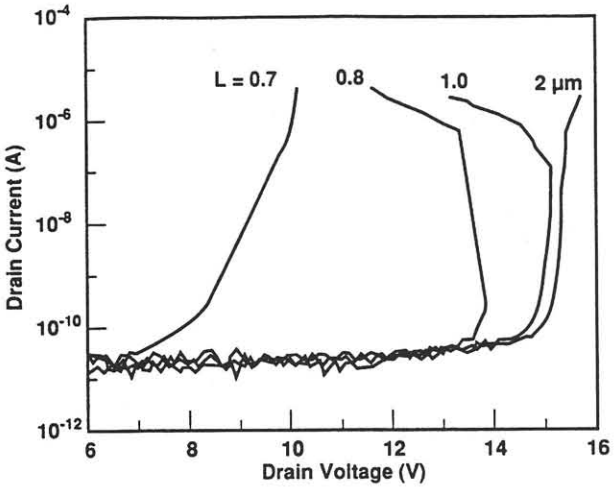

Fig. 3 I-V breakdown/snapback curve for L=0.7, 0.8, 1.0 and 2.0 μm.

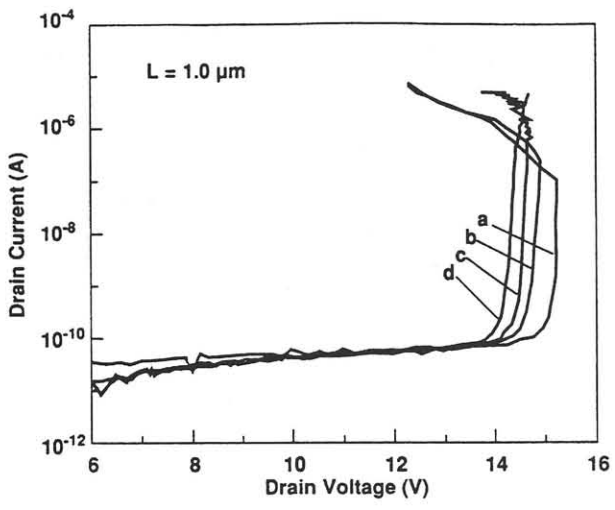

Fig. 4 I-V breakdown curve for different gate biases, (a)V_g=0, (b)V_g=-0.5V, (c)V_g=-1.0V, (d)V_g=-1.5V

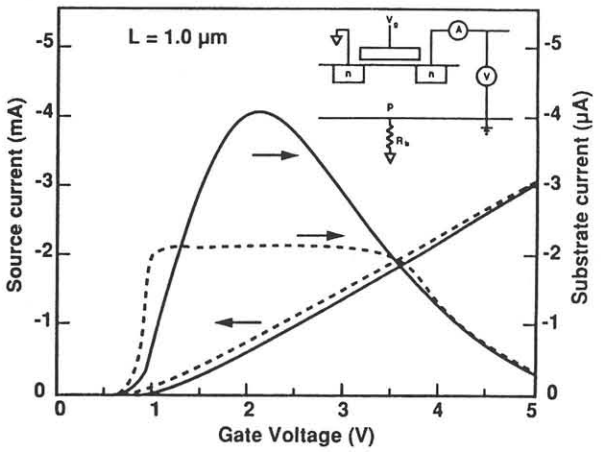

Fig. 5 Source and substrate current with (dashed) and without (solid) external substrate resistor R_b= 300 kΩ as shown in the insert.

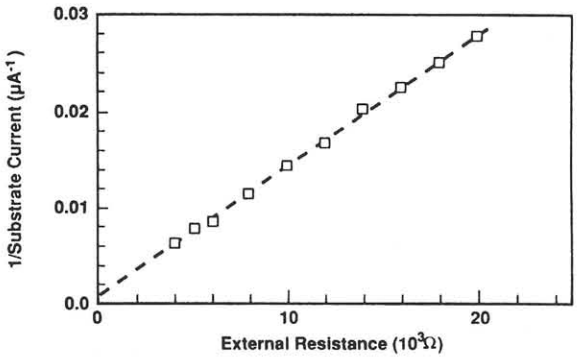

Fig. 6 1/Isub versus external substrate resistance

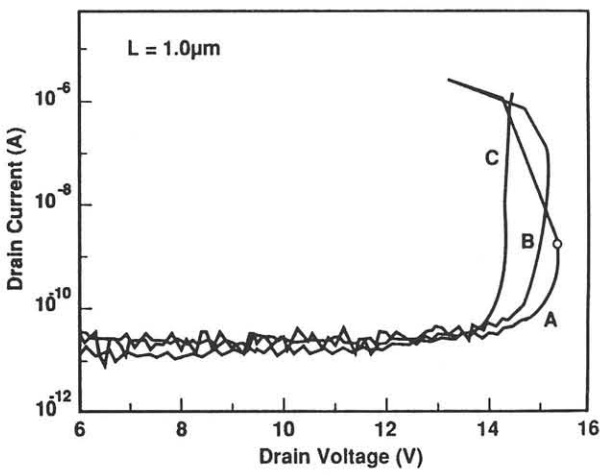

Fig. 7 I-V snapback curve for three different p well doses, A: 1.4E12/cm^2, B: 2.5E12/cm^2, C: 1.0E13/cm^2