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Structural, Chemical and Electrical Properties of Si Wafers for ULSI Applications

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The morphology of Si surfaces has been investigated in a multi-technique approach from microscopic to atomic scale concluding that chemo-mechanical polishing and epitaxy produce nearly perfect surfaces. The chemical state of Si surfaces, however, depends on final cleaning and aging of the wafers.
During wafer processing this perfect structure deteriorates. The influence of oxidation, cleaning, etching, precipitation, ion and plasma treatments, and contaminations on morphology is demonstrated. The impact on electrical properties (mobility, interface states, dielectric breakdown) will be discussed.

1. INTRODUCTION

Very thin gate oxides in the range of a few nanometers are used in ultra large scale integrated circuits (ULSI). This requires high chemical purity, perfect crystalline structure, and the absence of bulk micro defects.
The chemical state of this top layer of a silicon wafer surface depends on many processing steps like sawing, lapping, etching, and in particular on chemo-mechanical polishing, epitaxy, and subsequent cleaning, which are the most sensitive final surface preparation steps in wafer manufacturing. The quality of this active device zone, however, has to be maintained through many device manufacturing steps in favour of yield optimizing.
This paper summarizes structural and chemical properties of Si surfaces, focuses on the interplay between both and demonstrates the impact on electrical properties. Particular emphasis is given on surface degradation during processing (fig.1).

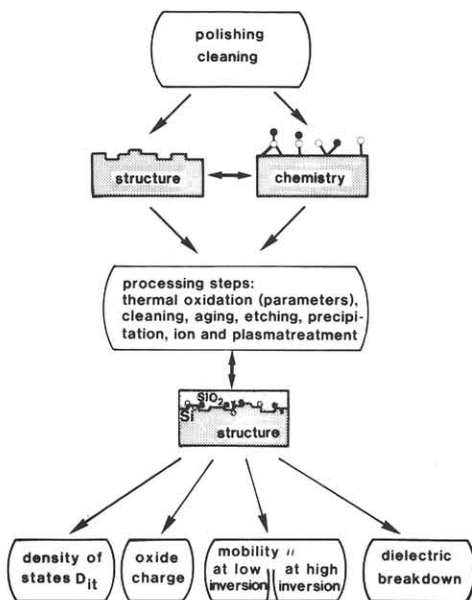

Fig.1: Combined influence of structural and chemical properties on electrical properties.

2. MORPHOLOGY OF SI-SURFACES

Modern lithography and stepper techniques demand very flat wafers. The geometrical properties are defined as "warp","bow", local (LTV) and total thickness variations (TTV).The LTV is specified for a site, which dimensions and numbers depend on wafer diameter.
Polishing is the final step to achieve surface smoothness. Long range undulations (macroscopic waviness) sometimes observed in polishing degrade LTV values. They are easily measured by profilometry , Normarski microscopy, interferometry, and the magic mirror [1] in particular. The latter moreover discovers defects like scratches, dimples, marks from prior treatments, orange peel, striations, and contours due to different attacks of the polishing slurry in a very fast and simple way. The perfection of polished silicon surfaces has been evaluated with LEED [2] (Low Energy Electron Diffraction) and STM [3] (Scanning Tunneling Microscopy) for Fourier components on an atomic scale.

The diffraction pattern of perfectly polished surfaces shows the 1x1 structure without any annealing. On purpose misoriented wafers show regular terraces with increasing regularity as polishing proceeds. The STM data provide additional insight into very local structures which are complementary to the LEED data.
Angle resolved lightscattering measurements (ARLS) confirm the smoothness of the polished surface covering sensitive distances from half the laser wavelength up to several tenth of microns depending on the scattering geometry.
A combined investigation of polished surfaces by ARLS and LEED measurements [4] demonstrates that an isotropic geometric distribution of atomic steps dominates the surface from atomic to micrometer scale.Both methods together yield a continuous description of the full range. Even the nonspecular amount of light is predictable by the electron diffraction data (see fig.2).

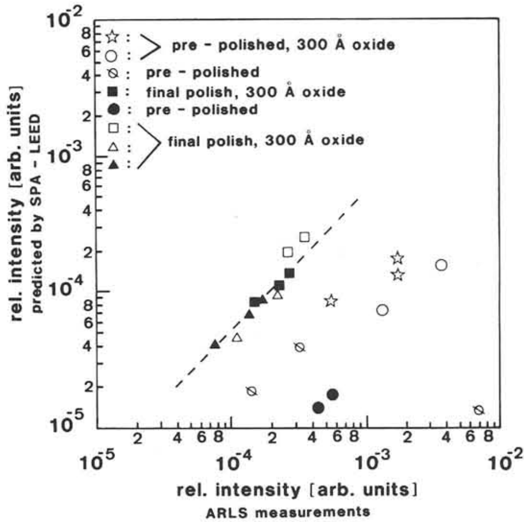

Fig. 2: Correlation of predicted (from LEED data assuming an isotropic geometric distribution of atomic steps) and measured ARLS-intensities [5]

The results show that all samples with a final polish are at the predicted intensity. All prepolished samples show a higher intensity than predicted. Obviously a lower intensity is impossible. This deviation may be caused by defects of different origin like polishing damage.
If the misorientation of the wafer under investigation is less than 0.1° the existence and regularity of the atomic terraces is proved by the lightscattering technique in complete analogy to the LEED-measurements. Under haze lamp inspection (a collimated beam of halogen light) this atomic grating decomposes white light into visible colours leading to "rainbow" haze. These wafers have the best surface in terms of smoothness. Consequently smoothness can be improved by using lightsattering as an in-line process monitoring tool.
In addition grazing incidence diffuse X-ray scattering measurements [5] were used to examine slightly misoriented samples. They were performed after deposition of 100nm Si by molecular beam epitaxy. Fig.3 exhibits

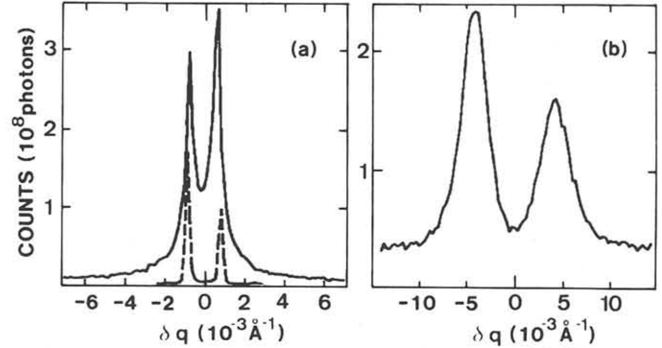

Fig. 3: Rocking scans through the (110) reflection of three samples showing atomic steps: The splitting distance corresponds to the miscut [5]

the rocking scans through the (110) bulk forbidden reflections of these samples. We again observe two distinct peaks. This doublet shows the existence of monoatomic, regular arrays of steps. The splitting distance confirms the small miscut (0.25°,0.04°,0.03°) leading to corresponding step separations (30nm,175nm,235nm).
Finally the atomic steps could directly be imaged on similar samples [6] with a scanning optical microscope (SOM 100 from Lasersharp).
These results show that the polishing procedures used in semiconductor wafer manufacturing produces nearly perfect samples. Only epitaxy can improve this quality further [2]. Thermal wave [10] measurements (information depth $\leq$ 3μm) demonstrate that this type of polishing does not introduce subsurface damage, too.

3. CHEMICAL STATE OF SI SURFACES

Polished silicon wafers show a hydrophilic behaviour after RCA cleaning or are hydrophobic as a consequence of a final HF dip. High resolution electron energy loss (HREELS) and x-ray photoelectron spectroscopy (XPS) measurements showed [7] that the hydrophilic property can be ascribed to Si-OH groups. On stored wafers these OH-groups can partially condense to Si-O-Si bridges leaving inhomogeneously distributed OH-groups on the surface. This structural change of the thin native oxide layer increases the scattered light. This effect if visible is well known as time dependent haze (TDH). This can lead to differences in oxidation rates and to a pronounced interface roughness [10].
Derivatization of the OH-groups, e.g. by a treatment with hexamethyldisilazane (HMDS),

stabilizes the surface and avoids this effect. Besides these structural differences surface contamination has an even more important influence on device yield. The present status and future needs are summarized in ref.[8].

4. PROCESS INDUCED DEFECTS

During subsequent processing steps, however, the perfection of the polished/epitaxial surface deteriorates in most cases again.

4.1 Thermal oxidation: Increase of roughness depends on oxidation parameters. A high quality oxidation minimizes this deterioration [2)9)10)].

4.2 Cleaning procedures: Different cleaning procedures lead to different surface states which again cause various degrees of roughening after oxidation. Cleaning with low concentrations of HF is known to cause surface roughening [2)9)10)].

4.3 Storage of wafers: During aging of wafers time dependent haze may occur causing enhanced interface roughness [2)9)10)].

4.4 Internal gettering: The benefit of precipitation may be counteracted by degradation of the surface caused by precipitates located directly at the surface in the formation of the "denuded zone" [2)9)10)].

4.5 Ion implantation and plasma treatment: Both treatments roughen the surface substantially and introduce subsurface damage, which is measurable by the thermal wave - and lightscattering technique [2)9)10)]. All these processing steps may deteriorate the smooth surface substantially. This degradation may only be minimized by proper process performance.

5. THE OVERALL INFLUENCE OF CONTAMINATIONS

Contaminations like heavy metals are of great concern in device processing. Their possible influence on material properties is demonstrated by the intentional contamination of the backside of the wafer by touching with a Cu,Fe, and Co wire. After oxidation and oxide removal the surface was evaluated by ARLS measurements. Fig.4 shows the corresponding roughness map [10)]. Cu and Co lead to a strongly enhanced roughness on the frontside of the wafer while Fe is not visible.
Similar investigations were carried out to show the influence of Fe and Cu on the minority carrier diffusion length by surface photo voltage measurements [10)]. Fig 5 depicts two SPV measurements using different wavelength (1000nm and 600nm). The Cu enriched at the surface is visible in any

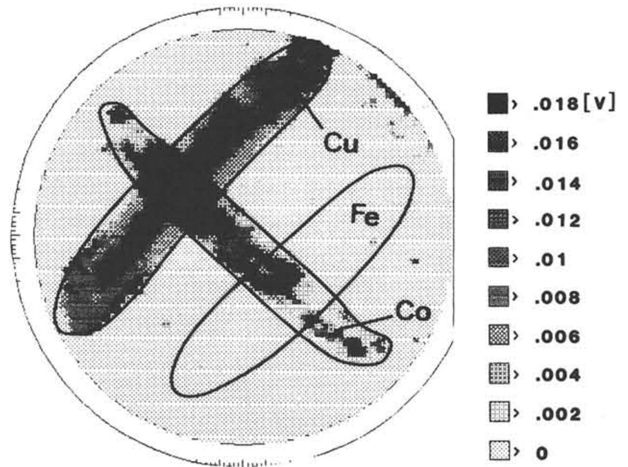

Fig. 4: Lightscattering map of the frontside of a wafer after oxidation and oxide removal. The wafer was contaminated with Cu, Co, and Fe as indicated on the backside before oxidation.

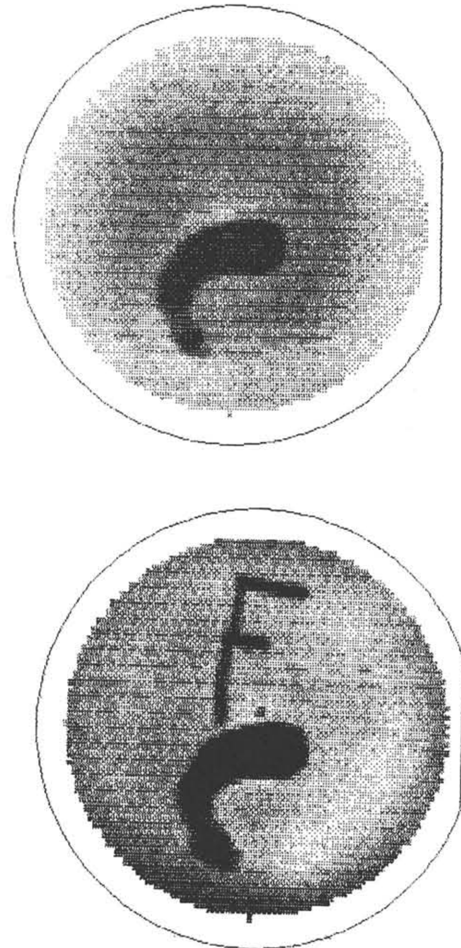

Fig. 5: Minority carrier diffusion length maps (after 10 min annealing at 1273 K) of a backside contaminated (Fe, Cu) wafer. The same wafer was measured (surface photo voltage) with different lightsources (600 nm upper, 1000 nm, lower picture).

case, but surprisingly Fe is only detectable using the longer wavelength which corresponds to an enhanced information depth. These data confirm the roughness measurements, Fe and Cu lead to microdefects or roughness directly at the interface.

6. CORRELATED ELECTRONIC PROPERTIES

For device performance not primarily the surface topography, but the correlation to electric parameters is of general concern. Fig.6 exhibits the possible influence of

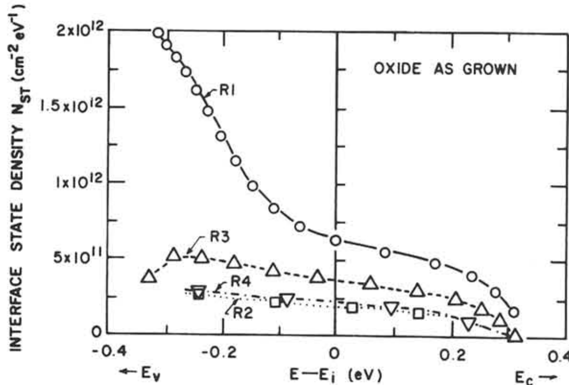

Fig. 6 Interface state density (N_{ST}) energy distribution for the transistors R1 (17%), R2 (8%) and R3 (21.2%), R4 (10%). Value in brackets is the step atom density (Si edge atoms per unit surface area). R1 and R2 as well as R3 and R4 were processed in one experimental run [11].

different interface roughness on interface state densities [11]. In this particular case we compared rough interfaces with even rougher ones, which explains the high densities shown.
Fig.7 shows the influence of the atomic

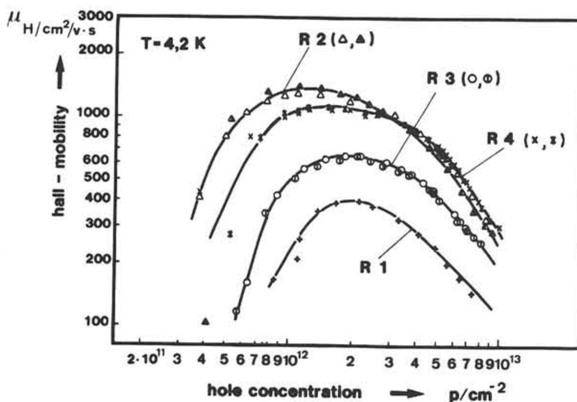

Fig. 7: Hall mobility vs hole concentration Samples have the same oxide thickness but different atomic step densities: R1=17%; R2=8%; R3=21%; R4=19%) [12]

roughness on the mobility in inversion layers [12]. At low inversion we observe an increase of the mobility due to coulomb scattering, and at high inversion a decrease due to roughness scattering. The product of atomic roughness and mobility at high inversion is constant approximately.
Fig. 8 demonstrates the influence of the

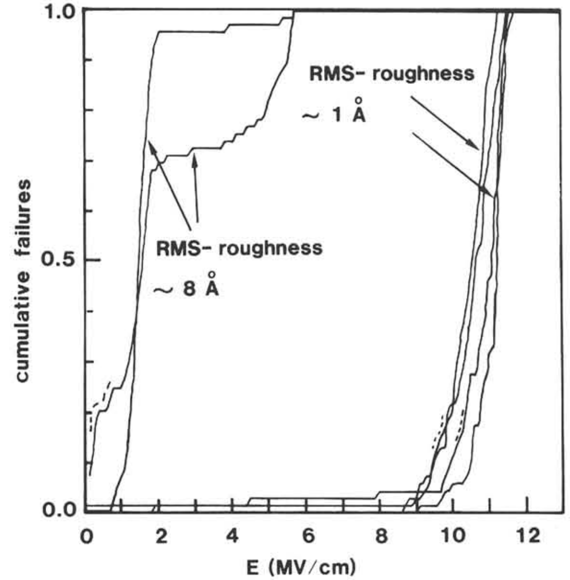

Fig 8: Influence of interface roughness on the cumulative failures of MOS capacitors [2]

microroughness (lightscattering) on the dielectric breakdown. Samples from an intermediate polishing step with a rough but damage free surface (as indicated by LEED and thermal wave measurements [10]) show very early intrinsic breakdown (1-2 MV/cm) values. After final polishing (RMS < 1Å) intrinsic breakdown fields at about 10-12 MV/cm are measured. An RMS value of about 5Å could be determined as a threshold. Beyond this limit the breakdown is reduced severely [10].

7. CONCLUSION

Chemo-mechanical polishing produces excellent surfaces with respect to atomic roughness (LEED) and microroughness (lightscattering). But most of the subsequent processing steps deteriorate the smoothness of the polished surface. Oxidation and etching may introduce surface roughness primarily. Precipitation,ion and plasma treatments may cause subsurface damage,too. Final cleaning steps gain more and more impact as shown by the influence of the structural change of the native oxide by condensation-hydratization processes. Summarizing, the results show that the electronic properties of MOS structures are very sensitive to the interplay of physical (structure) and chemical (cleaning) properties at the surface, interface, and during processing steps. Future demands underscore the necessity that more investigations have to be carried out.

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