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In-situ Multiprocessing ULSI Manufacturing Technology by RTP-CVD

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Future integrated circuits manufacturing will require a new class of equipment where large size single wafers are processed and several fabrication steps can be performed sequentially in the same equipment. The technique involves rapidly changing the wafer temperature and processing environment, and employing *in-situ* cleaning and *in-situ* process monitoring. The implementation of multiple *in-situ* processing steps within the same equipment has the potential to reduce particulate contamination and increase throughput, which should prove invaluable for ULSI manufacturing. Furthermore, each isolated process module can be integrated to match processing needs in an "application specific" fashion. In this paper, a novel single wafer multiprocessing technology, rapid thermal processing chemical vapor deposition (RTP-CVD), is described and experimental results are presented for *in-situ* deposition of semiconductors and dielectrics.

1. INTRODUCTION

As individual semiconductor device dimensions continue to shrink, stringent control over vertical profiles of layers and dopants on an atomic scale without sacrificing control of microscopic lateral dimensions over large areas is required. A key requirement is reducing thermal exposure to minimize dopant diffusion and interface broadening, complicated by the need for high processing temperatures to obtain higher deposition rates and epitaxial quality.

We have developed a novel single wafer *in-situ* multiprocessing technology, rapid thermal processing chemical vapor deposition (RTP-CVD), for multi-layer *in-situ* growth and deposition of dielectrics and semiconductors within a common processing chamber. By combining RTP with CVD, very short process times at high temperatures can be achieved, resulting in high quality epitaxy and good layer and dopant control with minimal thermal exposure.

2. SILICON EPITAXY

A schematic of the RTP-CVD system is shown in Fig. 1. The basic system concepts/designs are described in greater detail elsewhere[1]. We have grown high quality Si epilayers with hyper-abrupt interface transitions by RTP-CVD using SiH_2Cl_2 with H_2 as a carrier gas[2]. Heavily-doped p-type, (100)Si wafers were treated by a RCA clean. By performing the *in-situ* H_2 pre-clean at reduced pressure of 6 Torr, we can achieve epitaxy at growth temperatures ≥900°C using a pre-clean at 1000°C for less than 1 min.

Abrupt dopant transition profiles have numerous applications in ULSI technology. Fig. 2 shows the SIMS data for three epilayers of different thickness grown on heavily-doped p-type substrates at 1000°C. The drop in dopant concentration from 10^{18} cm^{-3} to 10^{16} cm^{-3} takes place in less than 400 Å, indicating a significant reduction of autodoping. Fig. 3 shows the SIMS profile for a multi-layer $p^-/p^+/p^-$ structure. Again, the dopant transition profiles are very sharp.

3. Ge_xSi_{1-x} EPITAXY

Recently, relaxed and strained Ge_xSi_{1-x} epitaxial alloy layers have received considerable attention. Strained Ge_xSi_{1-x} layers offer the ability to tailor the energy band gap by varying the Ge concentration, and the band alignment by using relaxed Ge_xSi_{1-x} layers. We have grown both strained and relaxed Ge_xSi_{1-x}/Si films in single and multiple layers using SiH_2Cl_2 and GeH_4[2-3]. Strained films were grown up to x≈13% at 900°C. The only defects observed were Ge interstitial loops confined near the heterointerface.

Figure 4 is a plane view TEM micrograph of a Ge_xSi_{1-x} layer grown at 1000°C showing a misfit dislocation network aligned along <110> directions and confined near the interface. Threading dislocations can be observed at the ends of some misfit dislocations. The total number of threading dislocations is small, indicating that the misfit dislocation propagation velocity is very high at the growth temperature of 1000°C. XTEM micrographs

show excellent surface and interface planarity, with a films thickness of 3380 Å. RBS depth profiles show good compositional uniformity with x≈7%. In comparison, we have observed Ge pile-up at both the surface and interface of relaxed films grown at 900°C with high threading dislocation densities.

4. SELECTIVE EPITAXIAL GROWTH (SEG)

Selective epitaxial growth (SEG) is emerging as a promising isolation technology for future ULSI because it offers very fine lateral and deep vertical isolation. SEG also has CMOS, bipolar, and Bi-CMOS applications. Problems associated with conventional SEG techniques due to thermal exposure include oxide sidewall undercutting[4] and high epitaxial defect densities along the sidewalls[5]. The reduced thermal exposure of RTP-CVD eliminates undercutting, improves selectivity, and reduces sidewall defects[6].

Lightly-doped, p-type (100)Si wafers covered with a 7000 Å thermal oxide patterned in <110> directions by RIE were used. An *in-situ* H_2 pre-clean at 1000-1150°C for 10-60s completely eliminated oxide sidewall undercutting while still maintaining an effective clean. For SiH_2Cl_2 volume concentrations in H_2 below 2%, excellent selectivity was achieved without adding HCl. Fig. 5 shows the growth rate vs. temperature. The activation energy in the surface reaction limited region is about 1.8 eV and the transition to the mass transport limited region occurs near 950°C.

The degree of faceting decreases with increasing growth temperature. For growth temperatures ≥1000°C, almost no faceting can be observed and the top surface looks smooth, but the oxide/epilayer interface contains numerous defects. At growth temperatures <1000°C, the oxide/epilayer interfaces are very sharp with no visible defects and the surface is smooth, but distinct faceting develops. We have identified {911} and {111} facet planes in addition to the common {311} facet planes.

5. *IN-SITU* DOPED SELECTIVE POLY-SI DEPOSITION

We have selectively deposited *in-situ* doped poly-Si as a diffusion source for shallow junction formation[7-8]. Using the same patterned substrates, excellent selectivity results similar to SEG were achieved. Fig. 6 shows an SEM micrograph of a sample processed at 800°C. The average poly-Si grain size is 0.03 μm at 775°C and increases to 0.2 μm at 850°C. Growth rate decreases with increasing doping levels. The inhibited growth has been attributed to preferential adsorption of the As species on the Si surface which saturates available adsorption sites and precludes the chemisorption and subsequent decomposition of SiH_2Cl_2.

The SIMS profiles in Fig. 7 show As pile-up at the surface and at the poly-Si/Si interface. The interface positions are consistent with XTEM results. The As pile-up at the interface indicates grain boundary segregation or impurity trapping of As near the interface. The As concentration increases with decreasing growth temperatures. SIMS profiles show the As concentration drops from 10^{19} cm^{-3} to 10^{17} cm^{-3} within 350 Å.

Dopant drive-in was performed by RTP at 1000-1100°C for 15-60s, resulting in partial alignment of the poly-Si and nonuniform breakup of the poly-Si/Si interface. The diffusion front is very uniform regardless of the nonuniformities in the poly-Si layer, indicating that the As rapidly and uniformly redistributes along the interface before diffusing into the substrate. Because dopant diffusivity is much lower in single-crystal Si than in poly-Si, subsequent movement into the substrate is limited and can be well-controlled to form very shallow damage-free junctions.

6. OXYNITRIDE AND NITRIDE GATE DIELECTRICS

Conventional thermal SiO_2 has difficulty in meeting the high quality, reliable, ultrathin (<100Å equivalent oxide thickness) gate dielectric requirements of ULSI MOS technology. Much attention has focused on stacked oxide/nitride/oxide (ONO) gate dielectrics due to superior performance and reliability. ONO combines the high interface integrity of SiO_2 with the higher dielectric constant and diffusion barrier properties of Si_3N_4. The top oxide significantly suppresses currents at high fields by reducing the hole injection from gate[9].

A process sequence of RTP-CVD of SiO_2 and Si_3N_4 layers followed by *in-situ* rapid thermal oxidation (RTO) in O_2 was used to fabricate ONO structures in the same chamber without breaking vacuum. SiO_2 was deposited at 11 Å/s by reacting SiH_2Cl_2 and N_2O at 800°C and 1 Torr. After a pump/purge cycle, Si_3N_4 was deposited at 4 Å/s by reacting SiH_4 and NH_3 at 700°C, resulting in a 60 Å nitride on top of a 100 Å oxide. RTO was performed at 1100°C for 60s at 1 atm in oxygen. AES depth profiles show well-defined ONO layers.

Fig. 8 shows the XPS spectra of the ONO films taken at various stages during Ar^+ sputtering. After 1 min, the Si 2p peak shifts to a lower energy, indicating the nitride layer has been reached since the Si 2p binding energy is higher in SiO_2 than in Si_3N_4. The peak shifts back to a higher energy after 3 min, indicating the bottom oxide layer has been reached. A second 2p peak appears after 12 min, indicating the SiO_2/Si interface has been reached since the Si 2p binding energy in pure Si is lower than that

in SiO_2. Only the peak from the substrate remains after 16 min.

We have also investigated the reliability of ultrathin (<50Å) nitride dielectrics in MOS capacitors. Devices with these nitride gate dielectrics have breakdown field larger than 17 MV/cm. Fig 9 shows a very high charge-to-breakdown (Q_{bd}) of 1000 C/cm^2, even for a high stress of -0.5 A/cm^2. A tighter breakdown distribution was obtained with a higher NH_3/SiH_4 ratio.

7. CONCLUSIONS

In summary, we have discussed a novel single wafer *in-situ* multi-processing technology, RTP-CVD, and have demonstrated its significant capability of multi-layer *in-situ* growth and deposition of dielectrics and semiconductors within the same processing chamber. In addition, selective deposition and *in-situ* doping of high quality Si epilayers with hyper-abrupt interfaces have been demonstrated. Due to a low thermal budget and processing flexibility, RTP-CVD will have a great impact on the next generation IC manufacturing.

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8. REFERENCES

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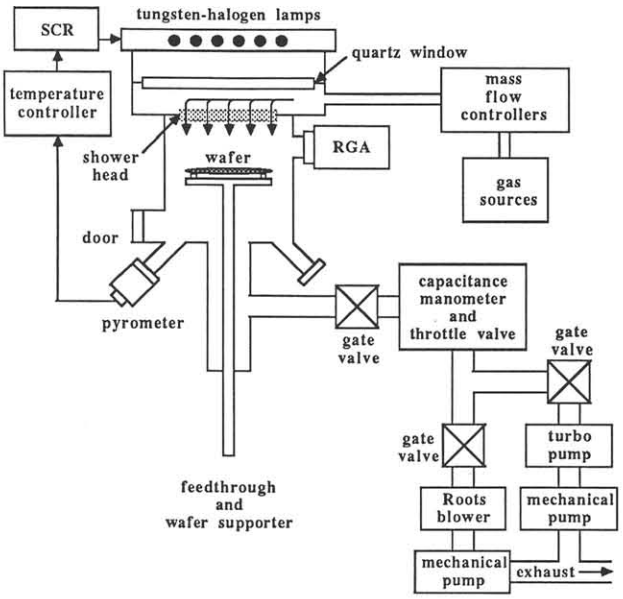

Fig. 1: Schematic diagram of a RTP-CVD system.

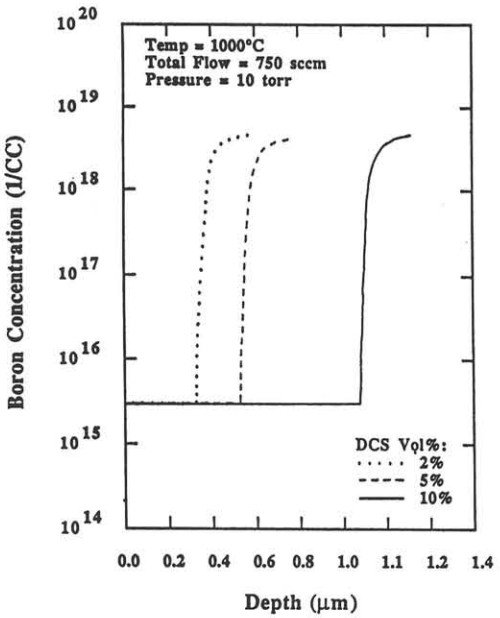

Fig. 2: SIMS profiles for undoped Si epitaxial layers grown on p^+ substrates at 1000°C.

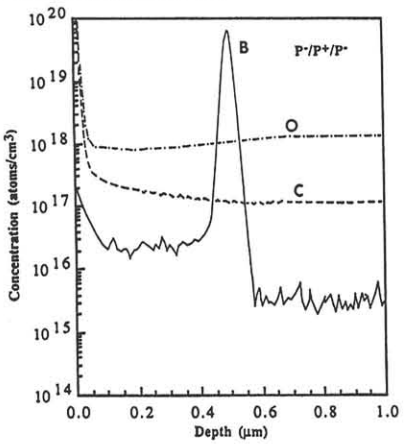

Fig. 3: SIMS profile for doped multi-layer structure.

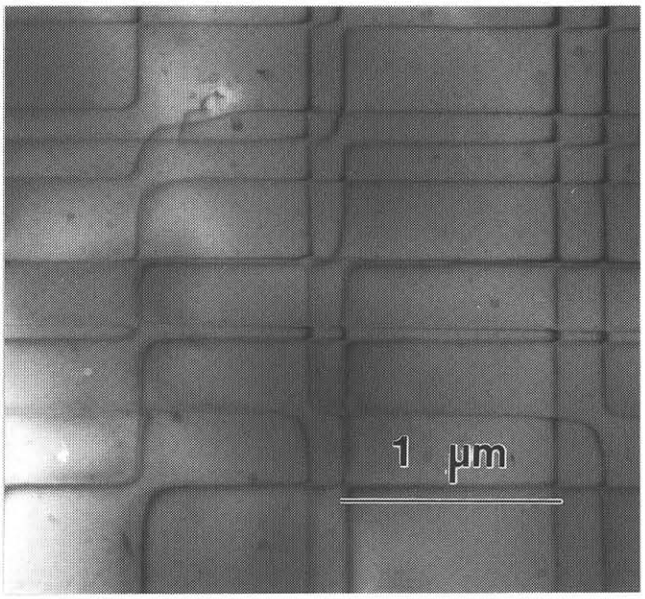

Fig. 4: Plane view TEM micrograph of Ge_xSi_{1-x} layer.

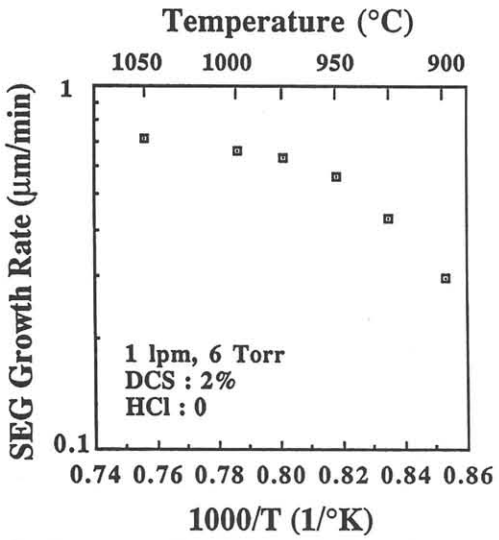

Fig. 5: Temperature dependence of SEG growth rate.

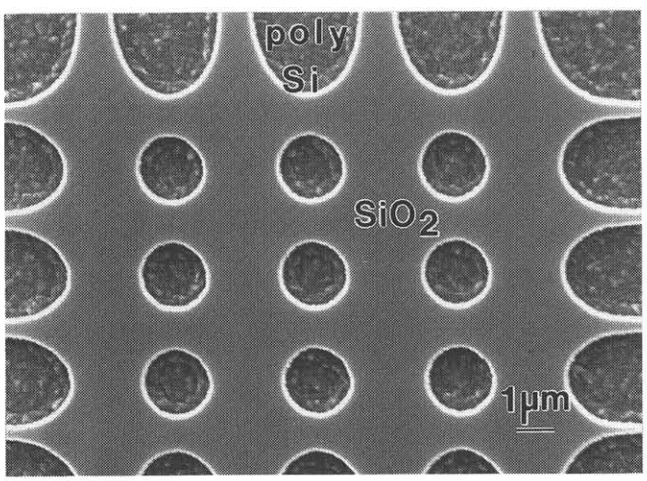

Fig. 6: SEM micrograph showing the top view of poly-Si contacts after 800°C deposition.

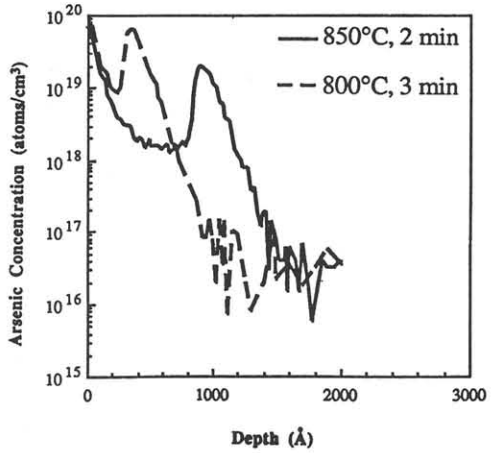

Fig. 7: As concentration profiles of samples from 2% vol SiH_2Cl_2 and 2 ppm AsH_3.

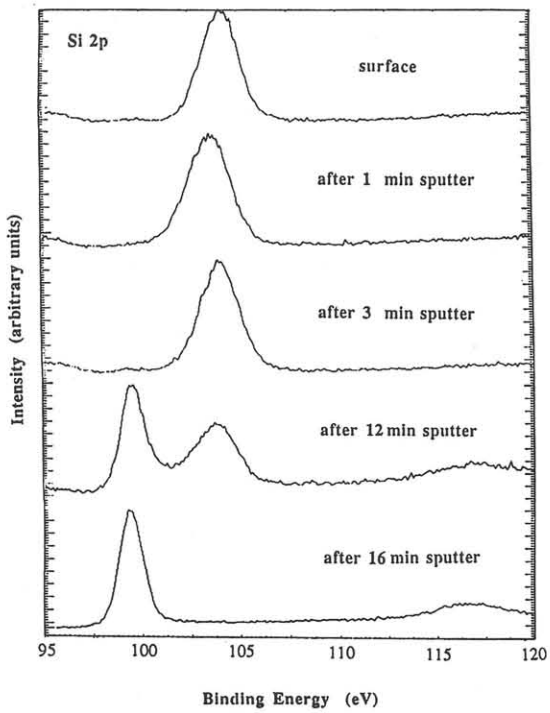

Fig. 8: XPS spectra of Si 2p taken at various stages of Ar+ sputtering of the ONO layer.

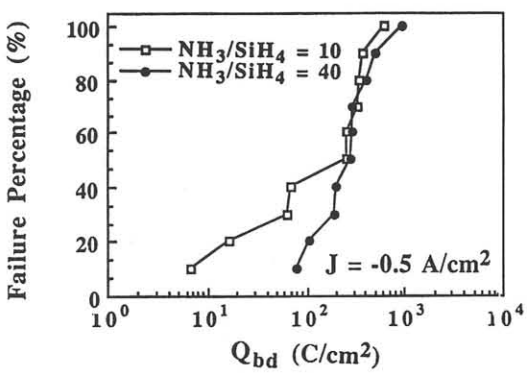

Fig. 9: Charge-to-breakdown of MOS capacitors with nitride as gate dielectric (equivalent oxide thickness is 50 Å).