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The Impact of Avalanche Generation on Punchthrough in Thin-Film SOI MOSFETs

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The punchthrough phenomena in thin-film SOI MOSFETs is examined using a two-carrier device simulator. Holes generated by impact ionization in thin-film SOI MOSFETs significantly degrade punchthrough resistance. Therefore, an LDD structure that decreases the electric field near the drain is effective in reducing the short channel effect in thin-film SOI MOSFETs. Thinning SOI film thickness and back gate oxide thickness enhances the front and back gate controllability. However, this is a trade-off for an increased electric field.

1. INTRODUCTION

The conventional SOI MOSFETs have advantages such as radiation resistance, latch-up free, and reduction of parasitic junction capacitances. However, conventional SOI MOSFETs have suffered from such disadvantages as the kink effect, and the current overshoot effect [1]. Recently, in thin-film SOI MOSFETs, the disappearance of the kink effect and of the current overshoot effect has been reported [2]. Furthermore, it has been shown that thin-film SOI MOSFETs have attractive features such as high punchthrough resistance, high Gm, and improved subthreshold characteristics [3]. Therefore, thin film SOI MOSFETs have received much attention in VLSI applications.

However, this study reveals that the punchthrough resistance of thin film SOI MOSFETs is not always higher than for conventional MOSFETs. It was found that holes generated by impact ionization in thin-film SOI MOSFETs significantly degrade punchthrough resistance, using a two-carrier device simulator. Despite disappearance of the substrate floating effect, hole behavior is an important factor in determining the SOI characteristics.

The position of thin film SOI MOSFETs with the thicknesses of back gate oxide (Tbox) and SOI films (Tsoi) as parameters is shown in Figure 1. The Tsoi and Tbox are important parameters in investigating the characteristics of SOI MOSFETs. This paper focuses on the punchthrough phenomena in thin-film SOI devices, and hole generation effects are discussed from the view point of device structure.

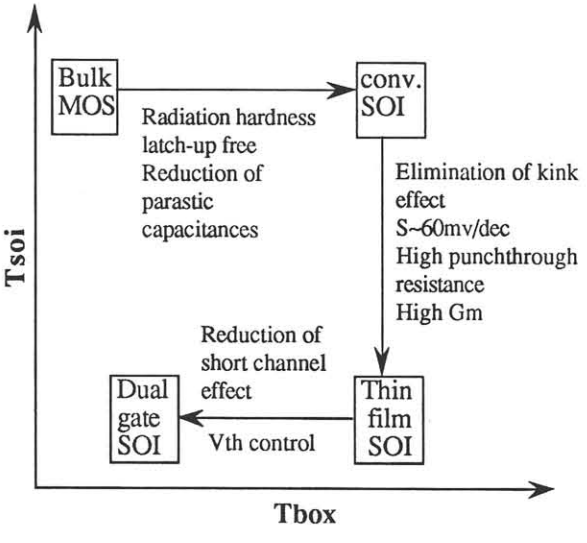


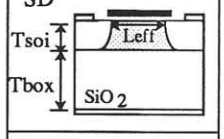
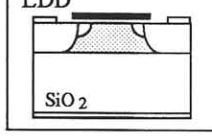
Fig. 1 The position of thin film SOI

2. ANALYSIS

The two-carrier device simulator, CADDETH [4], has been used to predict the characteristics in the subthreshold region.

The simulated device structure is shown in Table 1. The substrate of the device is doped with p-type impurities. The concentration is $1x10^{16}$ cm^{-3}. The gate material is n^+-polysilicon. The gate oxide thickness (Tox) was fixed at 10 nm. The range of the SOI film thickness (Tsoi) and back gate oxide thickness (Tbox) were varied from 0.02 to 0.2 μm and from 0.01 to 1.0 μm, respectively.

Table 1 Device structure

Device structure	Tox	substrate parameter			
		Tsoi	Tbox	Na	Xj
SD 	10nm	0.02μm ≀ 0.2μm	0.01μm ≀ 1.0μm	10^{16} / cm^3	0.05μm
LDD 		0.05μm	1.0μm		

3. RESULT & DISCUSSION

3.1 Punchthrough mechanism in thin film SOI

The dependence of punchhrough resistance on the number of electron-hole pairs generated by the avalanche effect due to impact ionization (Gaval) was investigated. The SOI film thickness (Tsoi) and the back gate oxide thickness (Tbox) were fixed at 0.05 μm and 1.0 μm respectively. The threshold voltage (Vth) at the drain voltages (Vd) of 0.1 V and 1.5 V, were simulated under the following conditions : 1) Avalanche generation is ignored. (Gaval=0), 2) Avalanche generation from impact ionization is computed by the following expressions (Gaval≠0)

$$Gaval = \frac{|Jn|}{q} An \exp\left(-\frac{Bn|Jn|}{E \cdot Jn}\right) + \frac{|Jp|}{q} Ap \exp\left(-\frac{Bp|Jp|}{E \cdot Jp}\right) \quad (1)$$

The ionization parameters (An, Bn, Ap, Bp) measured by Grant [5] were used in this work.

Results are plotted as a function of the effective channel length (Leff) in Fig. 2. At Vd=0.1 V the Vth-Leff characteristic does not depend on Gaval. At Vd=1.5V, calculation with Gaval≠0 result in a stronger short channel effect than with Gaval=0. The ΔVth1 in Fig. 2 is caused by holes generated by impact ionization. Figures 3 (a) and (b) show contour maps of the potential in SOI film in the subthreshold region (Vd=1.5 V, Vg=-0.4 V) with Gaval=0 and Gaval≠0, respectively. The potential computed with of Gaval≠0 is higher than the potential with Gaval=0. This is because almost all of the holes generated by impact ionization increase the potential in the substrate. This results in Vth-lowering. The ΔVth2 in Fig. 2 is caused by conventional potential-barrier lowering induced by the drain voltage. In the case of conventional MOSFETs, there was no difference between the two conditions, because the holes generated by impact ionization in MOSFETs flow out into the back gate. Thus, punchthrough in thin-film SOI MOSFETs is caused by two mechanisms. The first is the reduction of the source-to-substrate potential barrier from holes generated by impact ionization. The second is the conventional potential-barrier lowering induced by the drain voltage.

The Vth-Leff characteristics of a single drain structure are compared with those of an LDD structure in Fig. 4. It should be noted that the LDD structure has a higher punchthrough resistance than the single drain structure. This is mainly because the LDD structure reduces the electric field near the drain, resulting in less impact ionization.

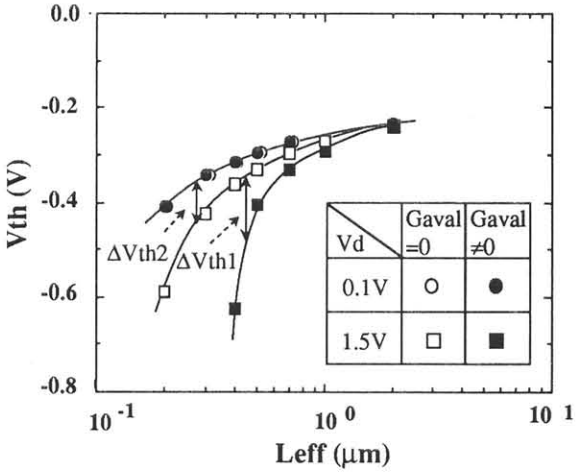
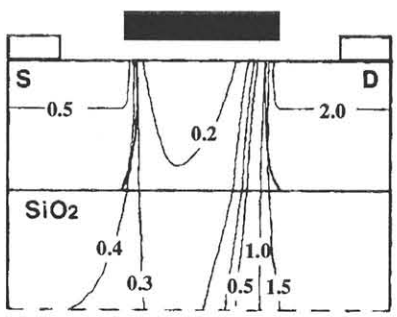
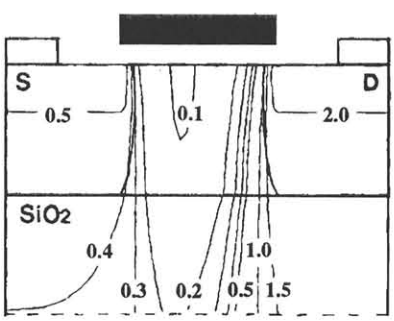


Fig. 2 Threshold voltage (Vth) of thin film SOI versus effective channel length (Leff) with Gaval and drain voltage (Vd) as parameters



(a) Gaval≠0



(b) Gaval=0

Fig. 3 Contuor maps of potential in SOI film with Gaval as parameter

3.2 Structure dependence of punchthrough resistance

Fig. 5 shows the dependence of Lmin on Tbox with Gaval as a parameter for a fixed SOI film thickness of Tsoi=0.05 μm. Lmin is defined as the channel length where ΔVth/ΔLeff=1 in Vth-

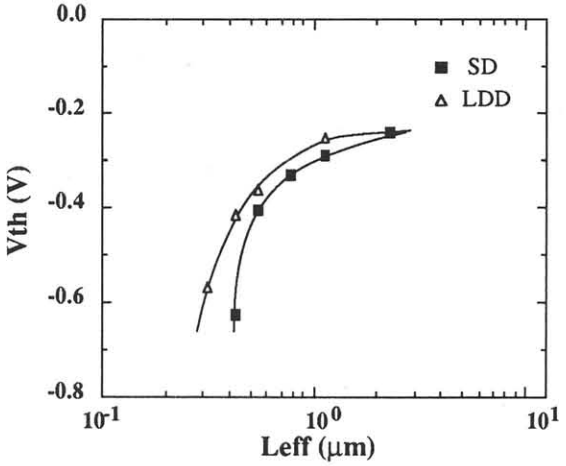


Fig. 4 Threshold voltage (Vth) of thin film SOI with SD and with LDD structure versus effective channel length (Leff).

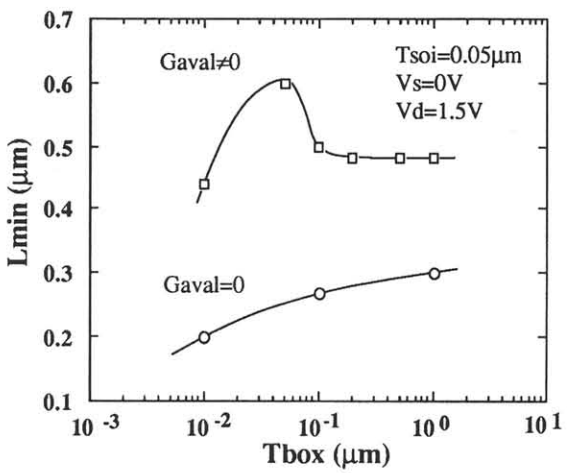


Fig. 5 Dependence of Lmin on Tbox with Gaval as paramter

lowering. With Gaval=0, Lmin decreases with Tbox, because back gate controllability is enhanced. On the other hand, for Gaval≠0, Lmin reaches a maximum. This is due to an increase in the electric field. Where Tbox > 0.05 μm, decreasing Tbox increases the electric field and the hole density, causing punchthrough. In the region of Tbox < 0.05 μm, Lmin decreases with Tbox, because back gate controllability enhancement is more effective than an increase in hole density. The dependence of the maximum electric field in SOI film (Emax) on the back gate oxide thickness (Tbox) is shown in Fig. 6.

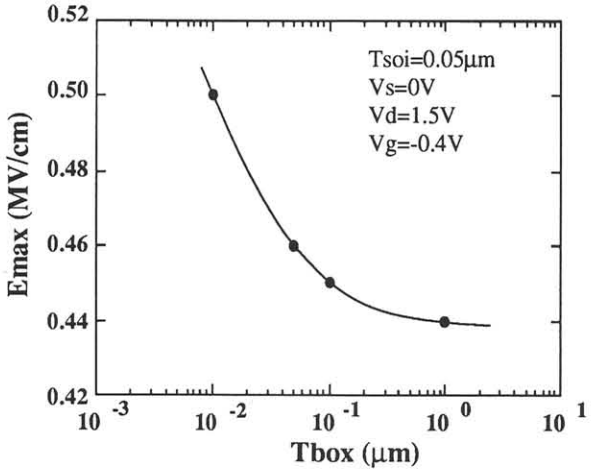


Fig. 6 The maximum electric field in SOI film (Emax) versus back gate oxide thickness (Tbox)

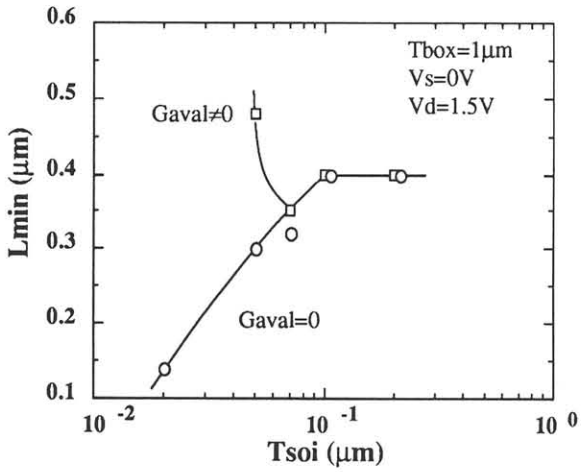


Fig. 7 Dependence of Lmin on Tsoi with Gaval as paramter

Fig. 7 shows the dependence of Lmin on SOI film thickness (Tsoi) with Gaval as a parameter for a fixed back gate oxide thickness of Tbox=1 μm. When Gaval=0, Lmin decreases with Tsoi. This is caused by front gate controllability enhancement. However, when Gaval≠0, Lmin has a minimum point. This is due to an increase in the electric field at the point where avalanche generation occurs. This happens when the electric current begins to flow near the gate where the electric field is high. Thus, a trade-off between front/back gate controllability and increase in the electric field occurs in the subthreshold characteristics of thin-film SOI MOSFETs.

4. CONCLUSION

Avalanche generation due to impact ionization in thin-film SOI MOSFETs significantly degrades punchthrough resistance. For that reason, an LDD structure that decreases the electric field near the drain is effective in reducing short channel effects in thin-film SOI MOSFETs. Thinning SOI film thickness and back gate oxide thickness enhance the front and back gate controllability. However, this is the trade-off for an increased electric field. Therefore, to have thin-film SOI MOSFETs with a 0.1μm channel length, it is necessary to find thin Tsoi and Tbox structures that are compatible with a reduced electric field.

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