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Ultra Thin Nitride Gate MISFET Operating with Tunneling Gate Current

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The electrical properties of ultra-thin nitride gates operating with large tunneling gate current have been demonstrated. Over all, drivability is very good. However, under low V_D and high V_G, most of the channel electrons tunnel into the gate, which reduces I_D. In the cut-off bias region, band-to-band current between the drain and the substrate is significant.

INTRODUCTION

A nitride film is regarded as a possible candidate for the ultra-thin gate insulator material in the next generation MISFET [1-5], because some silicon-nitride films have a low defect density, compared with that for silicon-oxide films, and the nitride film has a higher permittivity, which increases MISFET drivability. At the same time, very thin nitride films show larger tunnel leakage current, due to their smaller barrier height. In this paper, the electrical characteristics for ultra-thin nitride gate MISFETs are demonstrated. In addition, tunneling gate leakage current effects on the electric characteristics are discussed.

EXPERIMENTS AND RESULTS

N^+-poly-gate n-channel MISFETs and p^+-poly-gate p-channel MISFETs with ultra-thin nitride gate films were fabricated. The nitride film was formed directly on the silicon substrate by RTN (Rapid Thermal Nitridation). The physical thickness of the film measured by TEM was 25 A. Thus, equivalent thickness to the oxide film would be around 15 A. It should be noted that, in addition to nitrogen, significant amount of oxygen was detected in the film, which came from a native oxide layer at the silicon surface and/or very small amount of oxygen or water involvement in the RTN process. N^+-poly-gate n-channel MISFETs with a oxide gate film (30A) produced by RTO (Rapid Thermal Oxidation), were also fabricated as controls.

Figure 1 shows the I_D-V_D characteristics for ultra-thin nitride and oxide gate n-channel MISFETs. The nitride gate sample shows good characteristics. The nitride gate sample drivability was significantly higher, according to the large nitride gate film permittivity. A small concave in the V_D - I_D curve at high gate bias and low drain bias, is due to gate-to-drain tunnel leakage current. Figure 2 shows transconductance (g_m) dependence on gate bias. Very high g_m was observed for the nitride gate n-MISFET.

Figure 3 shows I_D, I_S, I_G, and I_{SUB} dependences on V_G at a) V_D = 0.05V, and b) V_D = 3V for the nitride gate n-MISFET.

First, a positive gate bias region is discussed. In the low V_D case (Fig. 3(a)), it should be noted that, under high positive gate bias, I_G becomes larger than I_D. The large I_G is the tunneling current of electrons from the entire channel region to the poly-Si gate as shown in Fig.4. Because most of the channel electrons were injected from the source into the gate, a smaller number of electrons reaches the drain. Thus, under high positive gate bias, I_D reduces with V_D, while I_S increases. The reduced I_D

under low V_D and high V_G can also be seen in Fig.1. Under this bias condition, I_D for the nitride gate sample is even smaller than that for the oxide gate sample. In the high V_D case (Fig. 3(b)), I_G reduces slightly from that in the low V_D case, because the electric field reduces between the channel and the poly Si near the drain.

Next, negative gate bias region is discussed. In the low V_D case (Fig. 3(a)), most of the electron tunneling current was injected from the gate to the substrate, the tunneling current component from the gate to the source/drain was small. This was clear from the fact that, in this bias region, the I_{SUB} curve overlaps the I_G curve and I_D and I_S curves are far below the I_G and I_{SUB} curve. In the high V_D case (Fig. 3(b)), band-to-band tunneling occurs between the drain and substrate. Current flow in this bias region is illustrated in Fig.5. The band-to-band current becomes the dominant component. The gate and source current components were minor.

Figure 6 shows the individual current component dependence on V_G for the oxide gate n-MISFET. I_G was very small, compared with that of the nitride gate, because the oxide film is about 5A thicker than the nitride film, and the nitride film barrier hight is lower than that for the oxide film.

Figure 7 shows nitride gate p-MISFET electric characteristics. In the low V_D case (Fig. 7(a)), a phenomenon similar to that for the n-MISFET case was observed, where, because of the large I_G, I_D decreases and I_S increases under high negative gate bias. In the high V_D case (Fig. 7(b)), under positive gate bias, band-to-band tunneling current between the drain and substrate (Fig.8) was observed. This band-to-band current was much larger than that for the n-MISFET. It has not been confirmed yet, but there is a possibility that n-MISFET gate film was thicker than that for the p-MISFET. It should be noted that drain to gate current (Fig.8) was very large. At $V_G = 0V$, it was even larger than the band-to-band current. The difference between the n- and p-MISFET gate-to-drain current might be due to some edge structure differences between n^+ and p^+ poly Si gates.

CONCLUSION

The electrical properties of ultra-thin nitride gates, operating with large tunneling gate current have been demonstrated. Over all, drivability is very good. However, under low V_D and high V_G, most of the channel electrons tunnel into the gate, which reduces I_D. In the cut-off bias region, band-to-band current between the drain and the substrate is significant for both the n- and p-MISFET cases. Tunneling current between the drain and gate should also be considered.

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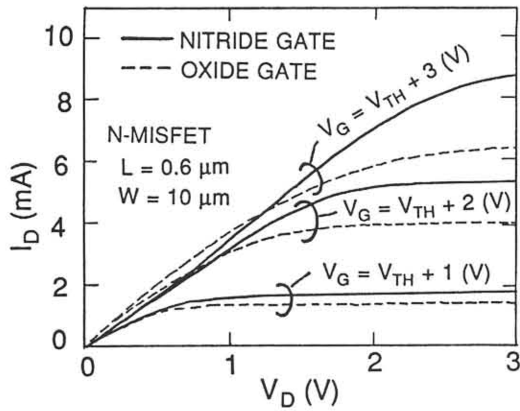


Fig 1. I_D-V_D characteristics for nitride and oxide gate n-MISFETs.

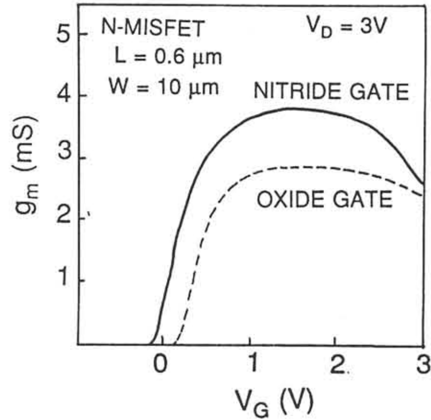
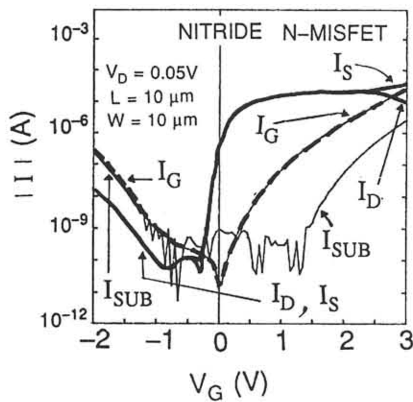
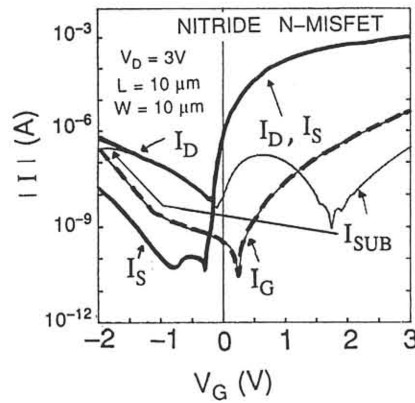


Fig 2. Transconductance dependence on gate bias



(a) Low V_D (0.05V) case



(b) High V_D (3V) case

Fig 3. I_D, I_S, I_G and I_{SUB} for nitride gate n-MISFET.

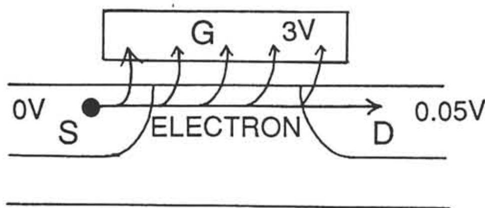


Fig 4. Channel electron current flow in nitrided gate n-MISFET, under low V_D and high V_G.

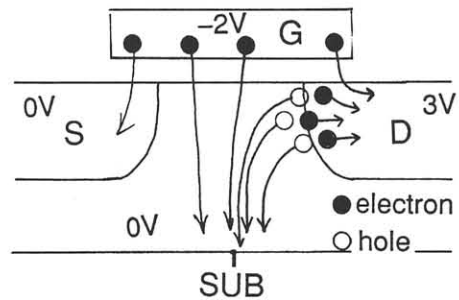
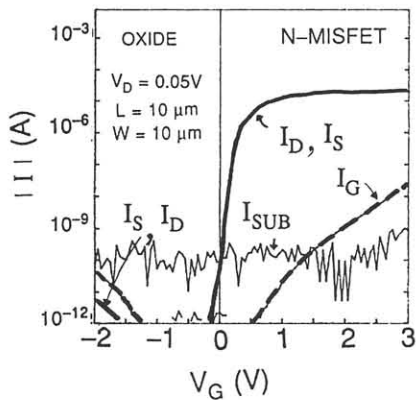
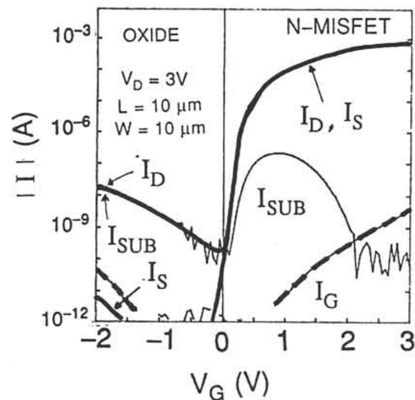


Fig 5. Carrier flow in nitride gate n-MISFET under cut-off gate bias region at high V_D.

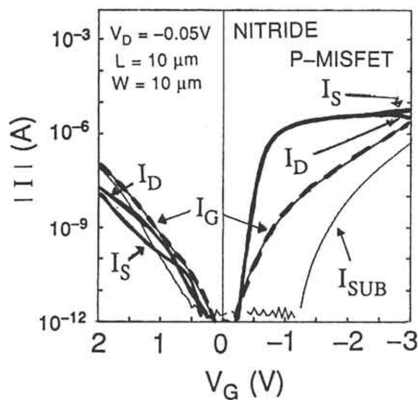


(a) Low V_D (0.05V) case

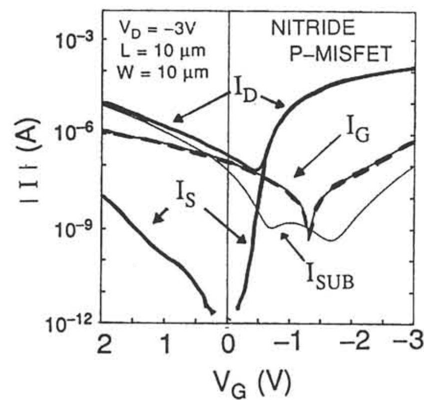


(b) High V_D (3V) case

Fig 6. I_D, I_S, I_G and I_{SUB} for oxide gate n-MISFET.



(a) Low V_D (−0.05V) case



(b) High V_D (−3V) case

Fig 7. I_D, I_S, I_G and I_{SUB} for nitride oxide p-MISFET.

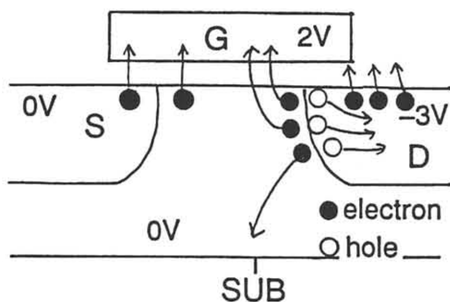


Fig 8. Carrier flow in nitride gate p-MISFET under cut-off gate bias region at high V_D.