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High Mobility Poly-Si Thin Film Transistor Fabricated in Avalanche-Nucleated Amorphous Si

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A poly-Si thin film transistor (TFT) with high field effect mobility is realized by using a poly-Si layer formed by a new method, avalanche nucleation of amorphous Si. Although the average grain size of the obtained layer is comparable to that of the conventional chemical vapor deposition method, the grains are aligned regularly to form a mosaic structure. This has lead to a potential barrier reduction at the grain boundaries. The obtained transistor (Lg/Wg=2μm/4μm) shows superior electrical characteristics such as high mobility (72cm^2/Vsec) and low subthreshold swing (104mV/decade). The results suggest the usefulness of the layer for fabrication of high drivability poly-Si TFTs.

1. Introduction

Recently, high mobility polycrystalline Si (poly-Si) thin film transistors (TFTs) have been attracting a great deal of attention. They are expected to be applied to liquid crystal display (LCD) drivers[1] and high density static random access memories (SRAMs)[2] *etc.* Several reports have appeared on the utilization of large grain poly-Si layers formed by solid phase growth of amorphous Si (a-Si)[1] and laser induced recrystallization[3]. In this paper, we will report for the first time that a high mobility of 72cm^2/Vs is obtained by using a poly-Si layer formed by a new method, avalanche nucleation of a-Si layer, even though the layer's average grain size is comparable to that obtained by the conventional CVD method.

2. Experimental

2.1 Poly-Si Layer Formation

P-type Si(100) (8-12Ω cm) wafers are covered with a 150nm-thick SiO_2 layer, which is arranged in a stripe pattern, by local oxidation of silicon (LOCOS). The wafers are then introduced into an ultra-high vacuum (UHV) chamber and their surfaces are cleaned by neutral Ar beam sputtering followed by *in situ* annealing at 680°C for 60min. Next, a-Si layer is formed on the sample by electron beam evaporation to a thickness of 600nm at a substrate temperature of 100°C. The pressure during the evaporation is kept at approximately 2×10^{-7}Pa. The layer is annealed *in situ* at 450°C for 60min to increase its density. This densification process is required to avoid indiffusion of impurities into the layer upon exposure to air[4]. After the wafers are unloaded from the chamber, their surfaces are cleaned using a mixture of NH_4OH, H_2O_2, and H_2O (1:1:2). Finally, they are annealed in an N_2 ambient at 600°C for 7h to induce avalanche nucleation for poly-Si layer formation.

The layer is evaluated by an optical microscope observation after the layer is Wright etched to delineate the grain boundaries. Trans-mission electron microscope (TEM) observations, both planar and cross sectional, are also carried out for evaluation of the layer.

2.2 TFT Fabrication

N-channel MOSFETs (nMOS) are fabricated in thus formed poly-Si layer. Prior to the fabrication, some samples are post-annealed in

an N_2 ambient at 1200°C for 12h to increase their grain sizes. Then, B-ions are implanted (25keV, $4x10^{12}cm^{-2}$) to make the poly-Si layer p-type for nMOS fabrication. The layer is etched off leaving an active area. MOSFETs are then fabricated by means of the conventional poly-Si gate nMOS fabrication process. The gate length and the gate width of the MOSFETs are varied between 1-10μm and 4-10μm, respectively. The gate oxide is thermally grown at 950°C to the thickness of 33nm.

3. Results and Discussion

3.1 Characteristics of Poly-Si Layer

Avalanche nucleation is a phenomenon in which nucleation rate of the a-Si is enhanced preferentially at the crystallization front and polycrystallization of the layer proceeds rapidly in the lateral direction[5]. As the poly-crystallization can be initiated by random nucleation of the a-Si, the stripe region is basically unnecessary in the growth.

However, in the experiment, the stripe region is utilized to define the location of crystal growth and to promote the onset of crystal growth in order to obtain the poly-Si layer in a shorter period. The a-Si layer first grows epitaxially in the vertical direction at the stripe region, where the layer is directly in contact with the Si substrate. Then, it polycrystallizes laterally on the SiO_2 from the stripe edge. The growth preferentially takes place at the edge of the stripe region. This may be due to that the stress localized in the vicinity of the region promotes random nucleation of the a-Si[6].

Crystal growth characteristics of the avalanche nucleation are shown in Fig.1. The solid phase epitaxial growth characteristics of the a-Si are also shown in the figure for comparison. The lateral growth velocity is found to exceed $6.9x10^{-7}$cm/s. This crys-tallization velocity is approximately 63 times higher than that of a normal solid phase growth

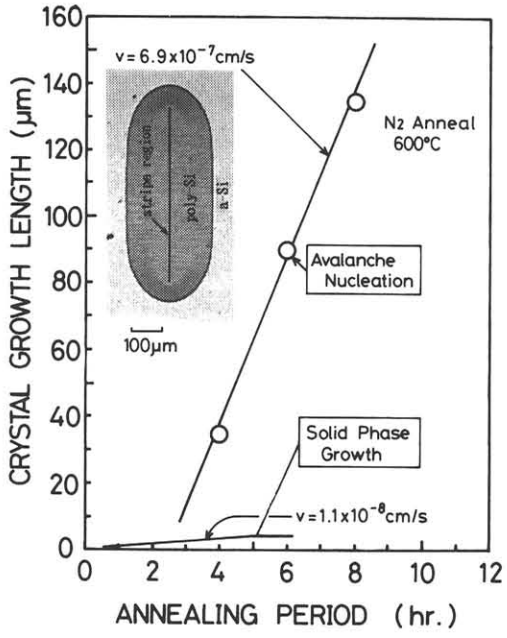

Fig.1 Crystal growth characteristics of avalanche nucleation. Inset shows optical micrograph of the sample after Wright etching.

($1.1x10^{-8}$cm/s). Optical micrograph of the sample surface after Wright etching is shown in the inset of Fig.1. As can be seen from the figure, a poly-Si layer of approximately 120μm is obtained as a result of the above mentioned N_2 annealing.

A transmission electron micrograph of the obtained poly-Si layer in the vicinity of the stripe region is shown in Fig.2. A single crystal is obtained at the stripe region and the poly-Si layer with a grain size of around 100nm is obtained in the region of the SiO_2 substrate. The obtained average grain size is comparable to that obtained by the conventional chemical vapor deposition (CVD) method. However, in the present case, all the grains have a columnar shape and are seen to form a mosaic structure. Moreover, vague grain boundaries are obtained.

A cross sectional view of the obtained layer is shown in Fig.3. As can be seen from the figure, the grain are also seen to form a mosaic structure in the vertical direction.

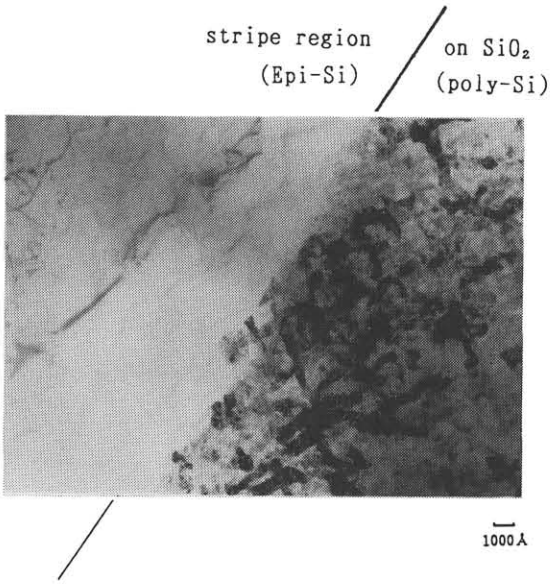

Fig.2 Transmission electron micrograph of the avalanche nucleated layer in the vicinity of the stripe region.

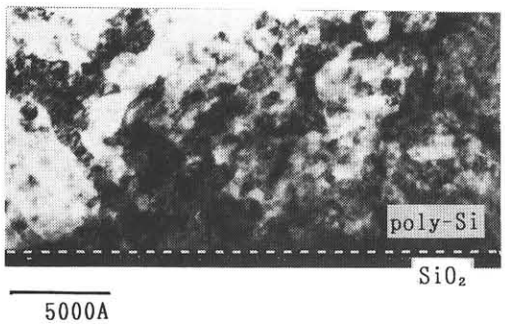

Fig.3 Cross sectional transmission electron micrograph of the avalanche nucleated layer.

3.2 TFT Characteristics

Drain current-drain voltage (Id-Vd) characteristics and subthreshold (Id-Vg) characteristics of the fabricated nMOSFET are shown in Figs.4 and 5, respectively. Gate length and gate width are 2μm and 4μm, respectively. The results indicate that the device is functioning normally. The leakage current is suppressed to pA/μm (Vd=3V) and due to low subthreshold swing of 104mV/decade, the on/off ratio of 5 decades is achieved with a 2V change in the gate voltage. Threshold voltage of 0.5V, which is close to that obtained from single crystal substrate, is realized.

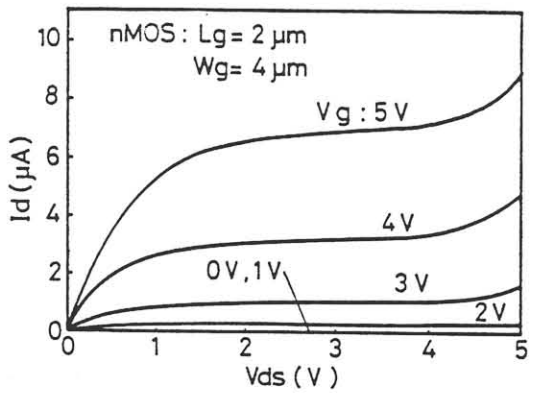

Fig.4 Id-Vd characteristics of the fabricated nMOS.

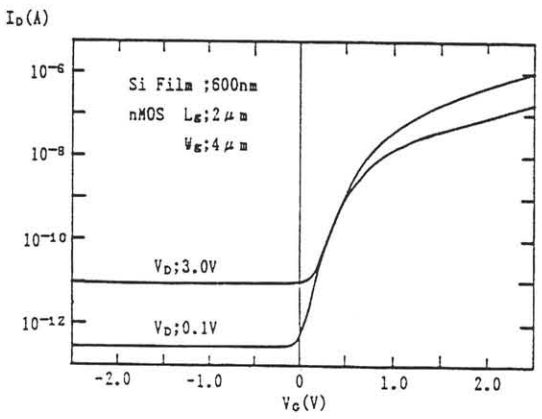

Fig.5 Subthreshold characteristics of the fabricated nMOS. A subthreshold swing of 104mV/decade is obtained.

As shown in Fig.6, transconductance (Gm) values of the obtained MOSFETs are plotted against the distance between gate center and edge of the stripe region. In the figure, the values obtained from both the as-grown poly-Si layer and the post-annealed layer are shown.

The value of Gm gradually decreases as the distance is increased. This result indicates that the polycrystallization takes place partly transmitting the information of the single crystal substrate. If there is an abrupt change in crystal structure at the stripe edge, a steeper reduction in Gm is expected.

Field effect mobility is deduced from the data shown in Fig.6. A high value of $72cm^2/Vsec$ is obtained for the MOSFET located the farthest distance away from the stripe. This value is found to increase to $485cm^2/Vs$ when the poly-Si layer is post-annealed at 1200°C for 12h prior to the device fabrication.

These superior electrical characteristics are attributed to the above mentioned crystal structure. The trap state density has been reduced as the columnar shaped grains are aligned regularly in the layer, and this has lead to a reduced potential barrier at the grain boundaries. The fact is also confirmed by the gate voltage dependence of the mobility. The mobility is found to have a peak value when the gate voltage is scanned.

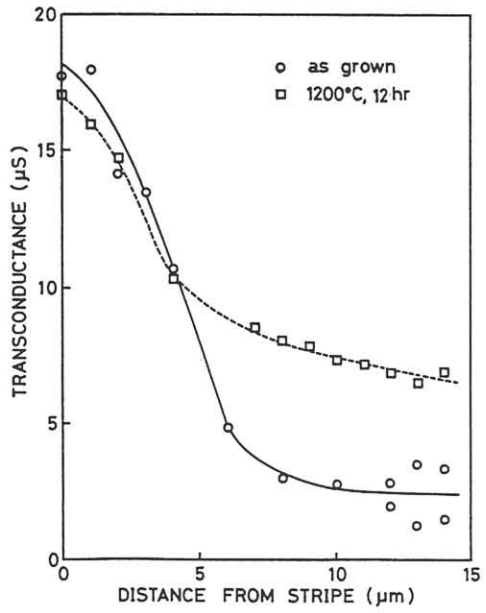

Fig.6 Transconductance of the fabricated MOSFETs as a function of the distance from the stripe edge.

4. Conclusion

Poly-Si TFT with high mobility has been realized by using a poly-Si layer formed by avalanche nucleation of a-Si. The results indicate the usefulness of the layer for fabrication of high drivability poly-Si TFTs.

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REFERENCES:

1) A.Mimura N.Konishi, K.Ono, J.Ohwada, Y.Hosokawa, Y.A.Ono, T.Suzuki, K.Miyata, and H.Kawakami, IEEE Trans. Electron Devices, ED-36 (1989) 351.
2) T.Yamanaka, T.Hashimoto, N.Hashimoto, T.Nishida, and Y.Kawamoto, Technical Digests of IEEE IEDM, San Francisco, Dec. 1988, p.48.
3) T.Serikawa, S.Shirai, A.Okamoto, and S.Suyama, IEEE Trans. Electron Devices, ED-36 (1989) 1929.
4) S.Saitoh, T.Sugii, H.Ishiwara, and S.Furukawa, Jpn. J. Appl. Phys., 20 (1981) L130.
5) M.Moniwa, M.Miyao, and T.Warabisako, Extended Abstracts of the 47th Autumn Meeting of the Japan Society of Applied Physics, Hokkaido, Oct. 1986, p.491.
6) M.Moniwa, M.Miyao, R.Tsuchiyama, A.Ishizaka, M.Ichikawa, H.Sunami and T.Tokuyama, Appl. Phys. Lett. 47, 113 (1985).