Leakage Currents Reduction of Poly-Si TFT’s by Two Step Annealing

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Leakage currents of polysilicon TFT’s were reduced significantly by a two step annealing technique which utilized low temperature crystallization of amorphous films and a reduction of trap states by a high temperature process. Trap state densities obtained from TFT’s on-currents correlated strongly with the leakage currents of TFT’s fabricated under different TFT processes.

1. Introduction

Leakage currents reduction of polysilicon TFT’s is critical for achieving high precision and large area liquid crystal displays (LCD’s). High temperature process of more than 1000 °C does not necessarily insures sufficient reduction of leakage currents of polysilicon TFT’s (1). Leakage currents or off-currents are thought to originate from field emission of carriers through trap states in the grain boundaries of drain junction regions (2). To date, however, no experimental result has been reported about the relationship between trap densities and leakage currents of polysilicon TFT’s. About polysilicon films, increase in grain size is observed by low temperature crystallization of LPCVD amorphous films (3).

In this paper, we tried to decrease the leakage currents of polysilicon TFT’s by a two step annealing technique, where LPCVD amorphous films were first crystallized at a low temperature (600 °C) and then the grain boundary trap states were reduced by a high temperature (1000 °C) process. Significant reduction of leakage currents was observed for two step annealed TFT’s. Furthermore, it was found that trap densities calculated from TFT’s on-currents were correlated with leakage currents of polysilicon TFT’s fabricated under different TFT processes.

2. Experimental

LPCVD amorphous films (800 Å) were deposited at 550 °C on quartz substrates and they were crystallized at 600 °C for 20 hours in nitrogen ambient (4). Boron ions were implanted at a dose, \( \phi \), of \( 1 \times 10^{12} \text{cm}^{-2} \) to \( 6 \times 10^{12} \text{cm}^{-2} \) (20 keV) (5). After patterning of polysilicon islands, gate insulators (1000 Å SiO \(_2\)) were deposited by APCVD technique at 480 °C.
Gate electrodes were also deposited by LPCVD at 550°C. After source and drain formation, phosphorous ions were implanted at 20 keV (5×10^{15} \text{cm}^{-2}). Then, the samples were annealed at 1000°C for 1 hour for the purpose of impurity activation and of trap state reduction in grain boundaries. Finally, hydrogenation was done in a conventional plasma CVD reactor at 300 °C for 1 hour. Trap densities (N_t) were obtained from \ln( \frac{I_p}{V_o} ) - 1/V_o plots of TFT's on-currents (6). Electron spin densities were measured by ESR in the x-band at room temperature.

3. Results and Discussion

Fig.1 shows electron spin densities of polysilicon films which were annealed first at 600°C and then at different high temperatures for 1 hour. As the second annealing temperature increases, electron spin densities are reduced significantly. Without the first step annealing, electron spin densities give higher values (by about 20% under 1000 °C process). This implies that the two step annealing can reduce trap densities and thus leakage currents of poly-silicon TFT's.

Fig.2 shows TFT I_p - V_o curves obtained from 600 °C and 1000°C processes. The leakage currents (V_o = 0 V, V_D = 10 V) were reduced by nearly two orders of magnitude; field effect mobilities were increased from about 35 cm^2/Vs to about 50cm^2/Vs; threshold voltages were reduced from about 6 V to about 4 V.

Fig.3 shows the effect of boron concentration in the channel regions on the leakage currents for 1000 °C process. Minimum leakage currents were observed for boron doping at 1×10^{12} \text{cm}^{-2}. The minimum leakage currents are based on the reduction of the absolute leakage current levels rather than on the optimization of

![Fig.1 Electron spin densities of poly-silicon films crystallized at 600 °C and then annealed at different high temperatures. Direct anneal is shown by dashed line.](image1.png)

![Fig.2 I_p - V_o curves of TFT's fabricated under 600°C and 1000°C (two step anneal) processes.](image2.png)
the threshold voltages.

![Graph showing the effect of channel dose on leakage currents.]

**Fig.3** Effect of channel dose on leakage currents.

Fig.4 shows \( \ln(I_o/V_c) - 1/V_c \) plots from TFT on-currents. A linear correlation in the range of 5 V to 30 V of \( V_c \) implies a validity of a single energy trap level. High temperature and hydrogenation processes generally give gentle slopes which indicate small trap densities. Electron spin densities in Fig.1 seem to have a good relationship with trap state densities.

Fig.5 shows \( \ln(I_L/\phi) - 1/\phi \) plots for 1000 °C process TFT's (\( I_L \): leakage currents for \( V_c = 0 \) V, \( V_d = 0.1 \) V). The slope also gives a trap density if we assume that the channel doping does not affect the trap levels (6). This plot, however, gives a lower trap density than those from Fig.4 by nearly one order of magnitude. Leakage currents under small drain biases suggest to have poor correlations with trap densities.

Fig.6 shows a relationship between the leakage currents and the trap densities for different TFT processes. The leakage currents depend strongly on the trap densities. The reason for this strong dependence is thought as follows; the trap levels are assumed to be a single energy level, \( E_t \), however, the actual levels may be distributed around \( E_t \), and probably the low temperature(600°C) process produces
widely distributed energy levels. The high temperature (1000 °C) process can reduce not only the density at Et but the width of the trap level distribution. Then, the total midgap levels which influence the leakage currents might be reduced much less than the values in Fig.6.

4. Summary

Leakage currents of polysilicon TFT’s were reduced significantly by a two step annealing technique which utilized low temperature (600 °C) crystallization of amorphous films and trap state reduction by a high temperature (1000 °C) process. Leakage currents were also reduced by channel doping at 1×10^{12} cm^{-2} dose. Trap state densities obtained from TFTs’ on-currents correlated strongly with the leakage currents under different TFT processes.

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References