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# A High Density High Performance Cell for 4M Bit Full Feature EEPROM

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A new EEPROM cell structure is proposed, which achieves a high capacitive coupling ratio of more than 0.8 in a small cell size of 11.25 $\mu m^2$. The cell fabricated has sufficient cell threshold windows which extend to more than 5 volts and program cell current of more than 30 μA at program voltage of 14 volts. The cell endurance is more than $10^5$ erase/write cycles. Using this cell structure, a 4 mega bit full feature EEPROM of a high performance and high reliability can be acquired.

## 1. Introduction

Today, 1M bit full feature EEPROMs are available on the market. However, their capacity is not yet comparable with that of magnetic devices. To increase the capacity of EEPROM memory cards to be used as external data storage devices for computers, higher density and lower cost devices are still needed. For this purpose, we propose a new cell structure for 4M bit EEPROMs. The construction of a cell based on this structure requires a simplified process flow as compared with that for the 1M EEPROM cells[1][2] previously reported.

## 2. Process Technology

Process technology available for our cell uses a twin well, triple level polysilicon and double layers of metal, based on 0.6 μm CMOS process. A modified LOCOS isolation is used with a 600 nm thick field oxide adequate to 15 V programming voltage. The CMOS peripheral circuits have 15 nm gate oxides, an LDD structure for n-channel transistors and 30 nm gate oxides for high voltage transistors. Tunnel oxide is 8 nm thick and interpoly dielectric (oxide-nitride-oxide layers) equivalent thickness is 20 nm. Major process features are summarized in Table 1.

| Technology | Twin well CMOS<br>Triple level polysilicon<br>Double layers of Metal |
|---|---|
| Leff (min) | Nch 0.6μm<br>Pch 0.8μm |
| Fleld Oxide | 600nm |
| Tunnel Oxide | 8nm |
| Peripheral Gate Oxide | 15nm |
| High Voltage Gate | 30nm |
| Inter Poly Dielectric | 20nm (effective) |

**Table 1.** Key process features of the newly developed EEPROM.

## 3. Cell Structure

Previously we presented a cell, called SSTR cell, which has a floating gate sandwiched between two control gates for 1 mega bit EEPROMs[1][2]. This device contains a 30.4 $\mu m^2$ cell using a 1.0 μm lithography and a novel self-aligned tunnel region fabrication technology. In this paper,

an improved SSTR cell using a rather simplified process technology is proposed.

Figure 1 shows a schematic drawing of the top view and cross section of the proposed cell. The first polysilicon layer is used as the select gate and lower control gate, and these gates make a polysilicon window to form a self-aligned tunnel region. The tunnel region is merged with the

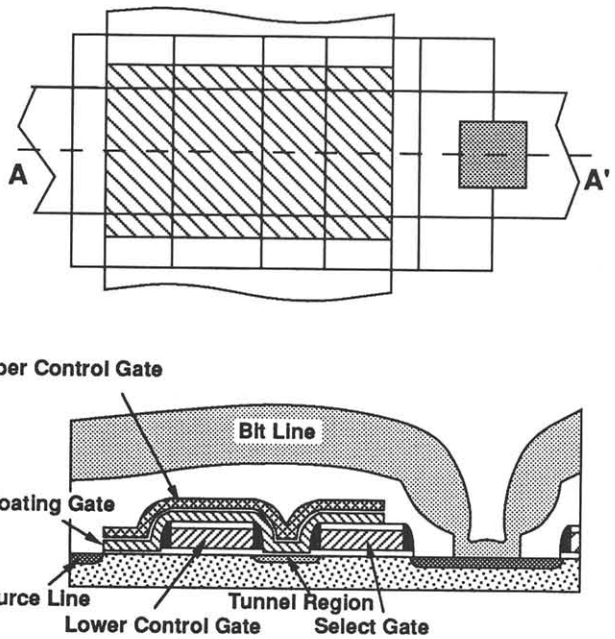


**Fig.1.** Schematic drawing of the newly developed cell. (a) Plane view (b) Cross section of A-A' of (a). The second aluminum layer is not shown for simplicity.

source region of the select gate transistor. Since the tunnel region lies between the select and lower control gates, its area is not affected by lithography registration. This suppresses the dispersion of the coupling ratio of the cell, which results in that of the cell characteristics. The peripheral gates are also formed by the first polysilicon layer. The second polysilicon layer forms the floating gate. The third polysilicon layer forms the upper control gate and is electrically connected to the lower control gate. The first aluminum layer is used as the bit line, and the second aluminum layer stitches the polysilicon word line to reduce the word line resistance for high speed performance. The select gate, tunnel region, control gate and floating gate are arranged in series between the bit line contact and the source line, without any dead space for margin for lithography registration. Due to the existence of the lower control gate, the capacitance between the floating and control gates of this cell is effectively increased. The capacitance between the floating gate and the substrate is decreased by the shielding effect of the lower control and select gates. The structural integration and advantages mentioned above enable this cell to achieve a small cell size of 11.25 $\mu m^2$ (2.5 $\mu$m X 4.5 $\mu$m) with a high coupling ratio of more than 0.8 using 0.6 $\mu$m lithography.

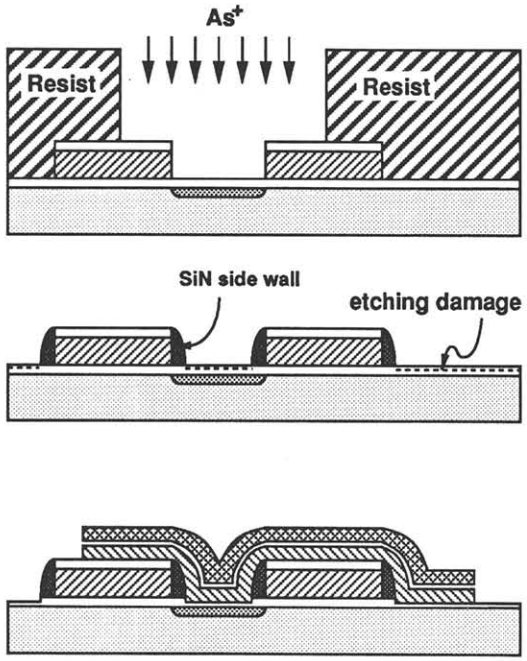


**Fig.2.** Key process sequence of the proposed cell.

## 4. Fabrication Technology

Figure 2 shows a major process sequence. After LOCOS isolation formation and gate oxidation, polysilicon and ONO interpolysilicon dielectrics are deposited. Then, the select gate and lower control gate are formed by RIE of these complex films. Subsequently, SiN side walls are

formed at the edges of the gates. While the SiN side walls prevent loss in thickness caused by HF treatment, break down voltage between the floating gate and the first polysilicon gate electrodes, i.e., select gate and lower control gate, is remarkably increased. Furthermore, etching process for SiN side wall formation has good selectivity to $SiO_2$, so that thin gate oxides on the active region of Si substrate can be used as an etching stopper, and RIE induced damages in the Si substrate are prevented by this $SiO_2$ stopping layer. This enables us to obtain highly reliable tunnel oxide despite the use of side wall etching process.

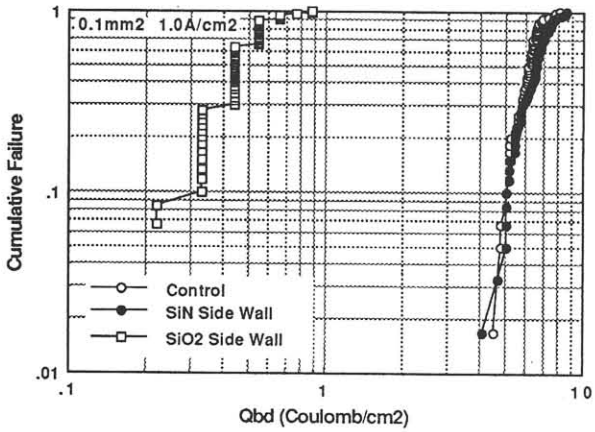


**Fig.3.** Constant current stress TDDB measurement of tunnel $SiO_2$ formed on the conventional $SiO_2$ and SiN side wall etched Si surface.

Figure 3 shows the tunnel oxide reliability measured by a constant current stressing test. Tunnel oxides are formed on the Si substrates of three different types. The first two are no damage induced substrate and conventional $SiO_2$ side wall etched Si substrate. The third one is SiN side wall etched Si substrate. The measured capacitor area is 0.1 $mm^2$ and current stress density is 1.0 $A/cm^2$ at gate positive biased condition. It is clear from the figure that SiN side wall etching process induces no damage to the Si substrate while conventional $SiO_2$ side wall etching causes serious degradation in tunnel oxide reliability.

After removing the damaged gate oxide (etching stopper) by HF treatment, tunnel oxide is thermally grown on the substrate. Then, the second polysilicon layer is deposited and etched to form the floating gate electrode. Later the interpoly dielectrics of ONO layers and the third polysilicon layer are deposited. The formation of the upper control gate and the successive formation of conventional contacts and aluminum interconnections complete the fabrication of the proposed cell. Figure 4 shows a cross sectional SEM micrograph of the finished device.

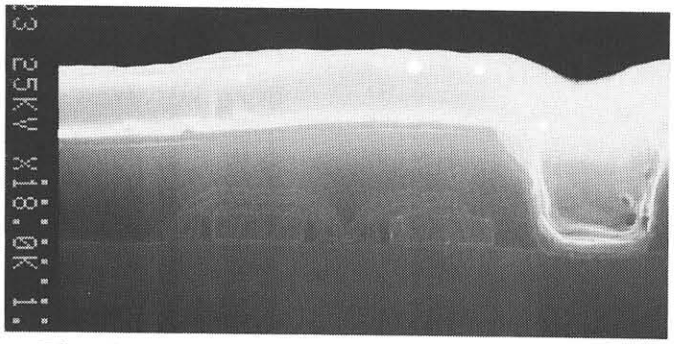

**Fig.4.** Cross sectional SEM micrograph of the proposed cell.

## 5. Cell Characteristics

The newly developed cell requires some bias voltage to the control gate in read operation, since it has an additional control gate transistor (lower control gate transistor). The conditions for various operations are listed in Table 2.

The program and erase characteristics of this cell are shown in Figure 5. The programmed state $V_{th}$ of the cell cannot be measured because of the existence of the lower control gate transistor as mentioned above. In the figure, the programmed cell characteristics are expressed by cell

| | Bit Line | Word Line | Control Gate | Source Line |
|---|---|---|---|---|
| Write | Vpp | Vpp | GND | Floating |
| Erase | GND | Vpp | Vpp | GND |
| Read | 1V | 5V | 3V | GND |

**Table 2.** Operational conditions for the proposed cell.

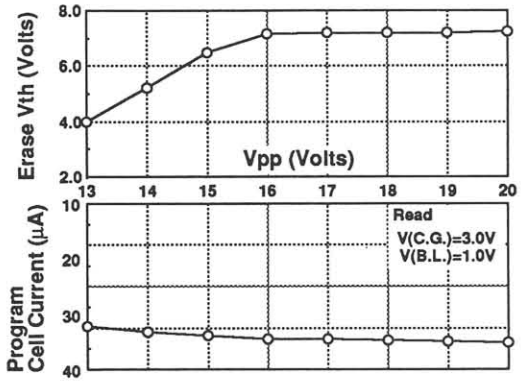


**Fig.5.** Erase/write characteristics of the proposed cell.

current under the select gate voltage of 5V, control gate voltage of 3V and bit line voltage of 1V. The erase $V_{th}$ is read as 5 volts and program cell current is 30 μA, yielding an acceptable threshold window, at a nominal programming voltage of 14 volts and pulse width of 4 msecs.

The single cell endurance is shown in Figure 6. It should be noted that rather different cell threshold window narrowing is observed. As the number of erase/write cycles increases, the value of programmed $V_{th}$ decreases for the case of conventional FLOTOX cells. This may be caused by the electron trapping in the SiN side wall at the source side edge of the lower control gate. Therefore, the thickness of the SiN side wall and that of the $SiO_2$ film under the SiN side wall might be optimized more carefully. Even without this optimization,

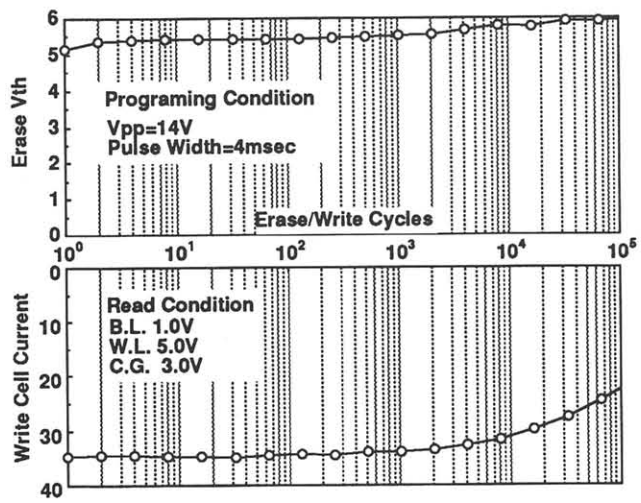


**Fig.6.** Endurance characteristics of the proposed cell.

our cell still attains the endurance of more than $10^5$ erase/write cycles, proving the validity of the SiN side wall formation process.

## 6. Conclusion

We have proposed a novel cell structure for a full feature 4 mega bit EEPROM. We have fabricated the cell that occupies only a small area of 11.25 $\mu m^2$ and attains a high coupling ratio of more than 0.8.

The cell can be programed with a programming voltage of 14V in both write and erase operations. The cell endurance of more than $10^5$ is obtained using the damageless SiN side wall process. The main feature of this cell structure is its very small cell size due to a self-aligned tunnel region formation. Using the currently available technology and the proposed cell structure, a high performance 4 mega bit EEPROM with high reliability is expected to be realized.

## 7. Acknowledgments

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## 8. References

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