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Limitations of Trench Cell Process Technologies for Submicron DRAMs

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New process features and process optimization details for the formation of DRAM cell storage nodes, transfer gates, and self aligned bitline contacts are presented for two types of stacked capacitor in trench cell concepts. Based on the proposed processes, 16M DRAMs have been fabricated and tested. In the light of the available data, critical requirements for 64M DRAMs are also discussed.

1. STORAGE NODE FORMATION & TRENCH ISOLATION

The application of the Stacked Capacitor in Trench Cell (STTC) for the fabrication of 16M and 64Mbit DRAM cells requires process optimization, particularly in regard to cell isolation. Two types of stacked capacitor cell are evaluated:

a) The storage node polySi electrode is deposited directly on the Si substrate inside the trench,[1], Fig.1

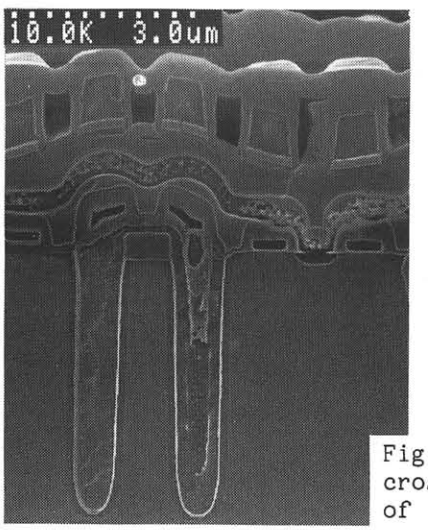

Fig.1 SEM cross section of 16M cell

Trench doping with very shallow junction depth (x_j = 0.45nm) is obtained by using in-situ As doped polySi deposition. Bulk Trench-trench leakage is suppressed by the adjustment of the p-well doping level for the cell array whereas surface leakage is suppressed by optimization of the channel stop implantation eg a high energy implant through the field oxide.

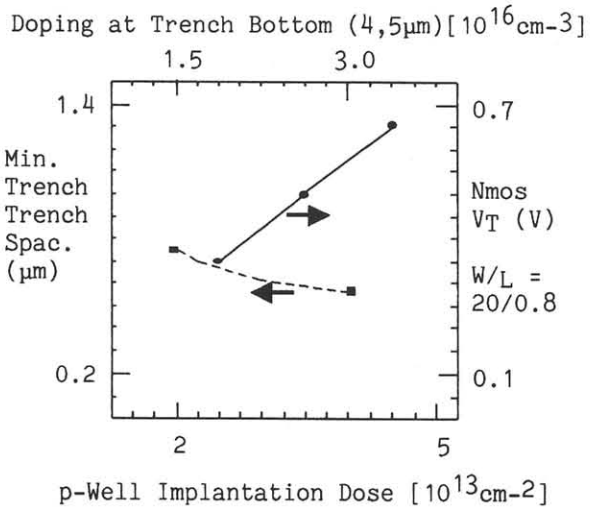

Fig 2 Min Trench-Spacing and n-Channel Threshold Voltage vs. p-well doping.

An upper limit to the p-well doping level is imposed by the generation of stacking faults during p-well drive in and by the fact that the threshold voltage of peripheral circuitry is targeted at 0.6V (Fig 2) with regard to circuit speed considerations.

Another possible leakage path for the STT cell is from trench diffusion to the bitline node. This leakage mechanism becomes critical for a trench to bitline node spacing of less than 0.6µm (Fig. 3) which allows for sufficient safety margin for 16M design rules (D.R's). For 64M design rules, suppression of trench- and trench to bitline node leakage require a modification of the cell structure.

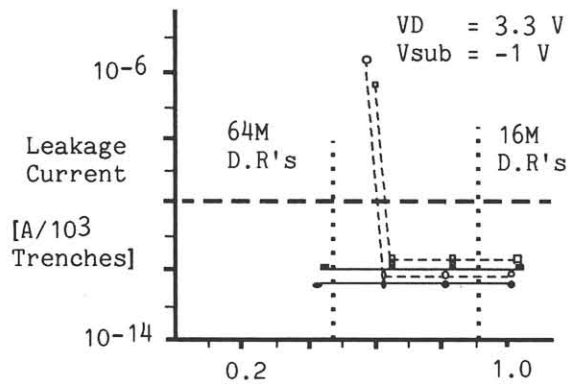

Fig.3 Trench to Bitline Leakage (□ ▮) and Trench to Trench Leakage current (o,●)for Stacked Trench (o,□) and Oxide Isolated Stacked Trench Cell (●, □).

b) The storage node polysilicon is isolated from the substrate by an oxide layer on the trench wall,[2]; The isolated Stacked Trench Cell, ISTTC. A buried trench contact at the trench sidewall adjoining active area connects the storage node to the transfer gate. Process and cell design rules are otherwise similar to the above.

Cell-cell leakage in this case is limited to that between adjacent buried contacts.

With quarter pitch bitline layout, adjacent contacts are offset and low leakage is observed down to 0.4µm trench-separation, Fig 3, fulfilling the requirements for 64M design rules. Variation in Trench contact depth (0.1 - 0.8µm) did not result in worsened leakage characteristics.

2. TRANSFER GATE TO TRENCH SEPARATION

The presence of the trench in the vicinity of the transfer gate may result in degraded subthreshold transistor characteristics, due to its possible influence on the source-channel potential hill height. Measurements of transistor Vt's and subthreshold slopes as a function of gate to trench separation remained, however, constant down to as drawn separations of < 0.1µm for the isolated storage node process (Fig.4). A sufficient tolerance for trench-transfer gate misalignment and trench enlargement at the 16M integration level is indicated.

Hot electron stress degradation measurements (Fig 5) showed additionally that the buried contact process does not significantly affect transistor lifetimes at small transfer gate to Trench separations.

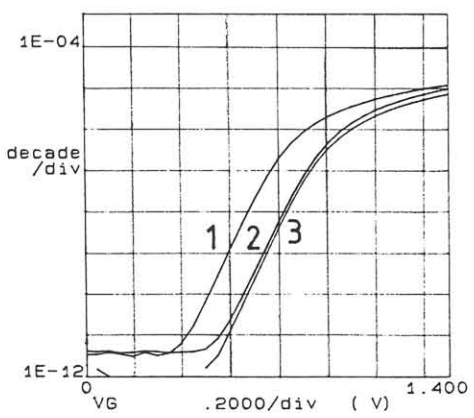

Fig.4 Dependence of subtreshold conduction on trench - transistor separation
1) 0.4µm
2) 0.2µm
3) 0 µm

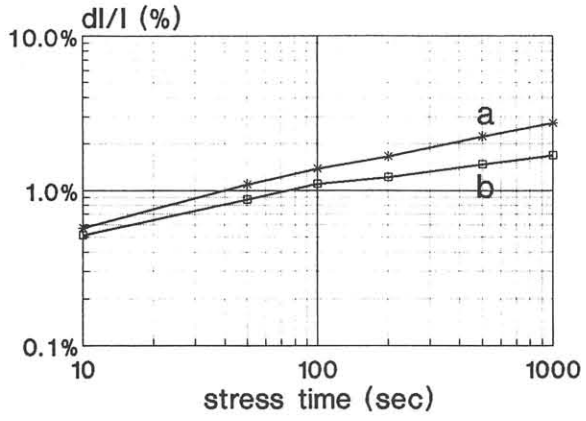

Fig.5 Dependence of Hot electron degradation on trench transistor separation.
Lg = 0,7µm, Vds = 8V, Vgs = 3V
a: Tr - Trans.: 0µm
b: Tr - Trans.: 0,4µm

3.SELF ALIGNED CONTACT TECHNOLOGY

The standard 4M FOBIC process 3), see Fig 6 offers limited capability for planarisation as increasing the thickness of the BPSG will necessitate increased wet etch times with associated extra undercut and consequent removal of BPSG within the region to be planarised.

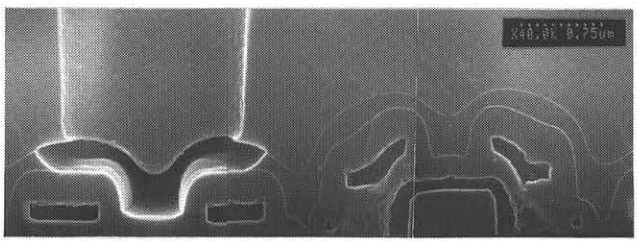

Fig.6 Cross Sectional SEM of the Standard FOBIC process perpendicular to the Word-lines.

An improved bitline contact technology is hence described, which avoids the wet etch, allowing thicker BPSG and consequently offers reduced topography. Field oxide protection is also enhanced with this process.
In Fig 7 a cross sectional SEM is shown of the new FOBIC where a nitride/polySi/BPSG-oxide multilayer allows contact window etch without significantly affecting gate

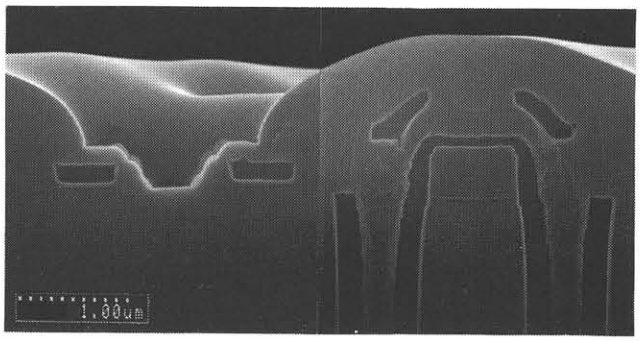

Fig.7 Cross Sectional SEM of the new FOBIC process perpendicular to the Word-lines.

or field oxide isolations. The BPSG film is etched anisotropically, using the 30nm polySi film as an etch stop. After polySi patterning and subsequent contact window etch it is wet oxidized with concurrent BPSG reflow. The underlying thin nitride acts as an oxidation barrier thus preventing undesired active area oxidation.

The complete oxidation of the polysilicon etch stop is one of the critical requirements for this technology. On planar areas, the oxide growth rate on polysilicon beneath BPSG is comparable to that on uncoated polysilicon. Retarded oxidation is observed between gate stacks with minimum spacing due to the reduced entrance angle for oxygen diffusion (as verified by a two dimensional process simulator). At concave corners residues are even more pronounced because of stress buildup during poly oxidation.

Since the source/drain junction depth should not be affected significantly, only a limited temperature budget for the polysilicon oxidation is allowed. Optimized processes yield complete polysilicon conversion, shallow source/drain junctions and good intermediate oxide reflow

planarisation at 850 - 900°C oxidation temperature.

4. 16M PROCESS

Using a 0.6µm twin well, triple poly, double metal CMOS process with the STT cell, 16M DRAMs have been fabricated (Fig 7). The chip is physically arranged in 64 blocks of 256kbit with 4 redundant rows and columns for each 512k block. Typical access time is 60nsec, and average power consumption is less than 500mW. A summary of the 16M DRAM parameters are given in Table 1.

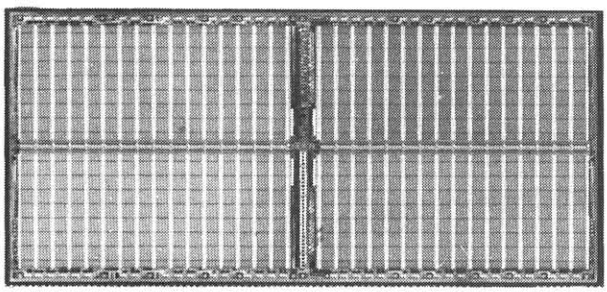

Fig.7 Photomicrograph of the 16Mbit DRAM.

5. CONCLUSION

Alternative cell technologies for 16M DRAM's are presented with additional critical design rule electrical data indicating their applicability to 64M DRAM's.

Table 1 16M DRAM parameters

Organization:	16M x 1, 4M x 4
Technology:	0.6µm p-subs Twin well CMOS
	35fF Stacked Trench cell
	Eff.Dielectric Thickness 9nm
	Transistor: Tox = 16nm,
	Ln/Lp = 0.8/0.9µm
	Triple Poly (1 Polycide),
	Double Metal
Cell size:	1.6µm x 3µm = 4.8µm^2
Chip size:	8.2mm x 17.7mm = 144.7 mm^2
Power Supply:	Ext. 5V, 3.3V in Cell Array

6. REFERENCES

1. Yoshikawa et al; Symposium VLSI Technology (1989) 67
2. Yoshioka et al; ISSCC Dig. Tech. (1987) 20
3. Küsters et al; Symp. VLSI Tech. Dig. (1987).93