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# Vertical Integration of an LED and a Vertical Transistor Using Selective MOCVD

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A GaAs vertical optoelectronic integrated circuit is fabricated using a selective atmosphere pressure MOCVD. It consists of a surface emitting LED and a vertical FET employing the embedded schottky contacts. As the drain current of the FET also flows through the LED structure, the light output of the LED is effectively controlled by the gate bias of the driver FET. This device operates as a three terminal optical device controlled by an electric input.

## I. Introduction

Many efforts have been made to develop optoelectronic integrated circuits (OEICs) because they have many advantages in performance, functionality and reliability[1]. Most efforts of OEICs are actually aimed at optical communication. However, they are also expected to be useful for the optical interconnection between boards and/or chips, and even within the chip. Recently, vertical cavity surface emitting laser diodes with high reflectance stacked mirrors has drawn attentions for various applications such as parallel signal processing and high speed optical interconnections[2,3]. Although the horizontal integration schemes are generally used, there are many problems to be overcome such as step coverage and device matching between electronic and optical devices. The fabrication process of the driver FET in an OEIC should be compatible with those of optical devices. The semiconductor-metal-semiconductor(SMS) structure can be used for the electronic device, particularly, the driver FET in OEIC. By fabricating optical devices on top of the SMS structure[4], the OEIC can be vertically integrated. The advantages of the vertical OEIC over those of the horizontal one are easy controllability of the optical output by the electronic input and the closer matching between the electronic and the optical parts. In addition, the vertical electronic devices such as PBT (or SIT) and vertical FET have smaller parasitics compared to the conventional MESFET used for horizontal integration and their operating frequencies become higher. In this paper we report the vertical integration of an surface emitting LED and a vertical FET employing embedded Schottky contacts.

## II. Device Fabrication

Figure 1 shows the schematic diagram of the fabricated vertical OEIC. The key structure of this device is a tungsten grating embedded into an epitaxial GaAs layer. The OEICs are made with the following fabrication steps. First, MOCVD is used to grow a ~1.0μm-thick n-GaAs on $n^+$ (100) GaAs substrate. Next the $SiO_2$ mask pattern which is used for the gate-pad area is formed. The thickness of the $SiO_2$ film deposited by RF sputtering is about 100nm. Conventional optical lithography is then used to define a 3μm-period grating pattern in AZ-5214 photoresist. This photoresist layer is used as a lift-off mask to pattern an RF sputtered tungsten film of 70nm thickness. The grating direction has an angle of 10-30° from the <011> direction on GaAs substrate. After cleaning in a sulfuric acid, 5 epitaxial layers are subsequently overgrown on the exposed region having tungsten gratings selectively by atmosphere pressure(AP) MOCVD. The V/III ratio is about 25 and the total flow rate is kept at 2.2 SLM. The growth rate is 0.04μm/min and the growth temperature is 650°C. The grown layers are FET channel layer (n-GaAs; undoped, ~2μm); lower cladding layer (n-$Al_{0.3}Ga_{0.7}As$; Si doped to $2\times10^{17}cm^{-3}$, 1μm); active layer (GaAs; undoped, 0.5μm); upper cladding layer (p-$Al_{0.3}Ga_{0.7}As$; Zn doped to $1\times10^{18}cm^{-3}$, 1μm); and cap layer ($p^+$-GaAs; Zn doped to $1\times10^{19}cm^{-3}$, 0.1μm). After the MOCVD growth, speckles of polycrystalline GaAs on the $SiO_2$ gate pad area are occasionally deposited. Those speckles are successfully removed by $HCl-CH_3COOH-K_2Cr_2O_7$ solution. After defining the active region by wet etching, the ohmic contact openings for the drain and the gate are formed on the PR mask. Au-Zn for the drain and the gate metallization is deposited at the same time. For N-ohmic metallization, Au/Ge-Ni is evaporated on the backside surface. Alloying is performed at 450°C for 2.5min.

## III. Results and discussions

For the device application, the surface morphology of the selectively grown layer should be smooth and flat. Lateral overgrowth on tungsten has also been found to be difficult to successfully accomplish using AP-MOCVD because the single crystalline deposition on tungsten gratings is very sensitive to the surface conditions. Also the dependence of the lateral overgrowth with tungsten grating orientation is strongly exhibited. A cross-sectional SEM photograph is shown in Fig.2. The triangular voids are shown above tungsten gratings. But, the precise effect of the voids has not yet been made clear. For the evaluation of the transistor we fabricate a mesa isolated vertical FET with $30 \times 30\mu m^2$ active region without LED layer. The characteristics of the FET can be divided into an pentode-like region and an triode-like region[5]. By varying the grating width and doping densities of the grown layers, we get two types mentioned above. The I-V characteristics of the pentode-like FET is shown in Fig.3. The doping concentration of the undoped GaAs layer is about $1\times10^{16}cm^{-3}$. The transconductance at $V_g=0V$ is $13.6mS/(30\mu m)^2$ and the threshold voltage is -2.1V.

Figure 4 shows the I-V characteristics of the driver FET in the proposed OEIC which has an the active region 110 × 150$\mu m^2$. Because of the close placement of an optical device and an electronic one, it is possible that the transistor action is affected by the emitted light. As we increase the magnitude of the gate bias, the drain current is abruptly increased. This phenomena may be due to the optoelectronic feedback. The light output versus $V_{DS}$ characteristics with $V_{GS}$ as a parameter are shown in Fig.5. With the gate voltage, the light output of the LED is readily modulated. But when $V_{GS}$ is reduced below -2V, modulation characteristics are degraded because they have a large leakage current and a breakdown voltage which is lower than expected. These degradations may be due to the crystal defect introduced at the interface between tungsten and GaAs during the process. Therefore, to improve these, the optimization of the process conditions is needed. This structure can be used to fabricate high power and high speed OEIC with a laser diode as an optical device.

## IV. Conclusions

A GaAs vertical OEIC which consists of a surface emitting LED and a vertical FET with SMS structure is fabricated using selective MOCVD. The close placement of an LED and an FET makes it easy to control the light output.

## References


1. S.R. Forrest, Proc. IEEE, 75 (1987) 1488.
2. J.L. Jewell, A. Scherer, S.L. McCall, Y.H. Lee, S. Walker, J.P. Harbison and L.T. Florez, Electron. Lett., 25 (1989) 1123.
3. Hoi-Jun Yoo, J.R. Hayes, N. Andreadakis, E.G. Pack, G.K. Chang, J.P. Harbison, L.T. Florez and Y.S. Kwon, Appl. Phys. Lett.,56 (1990) 1942.
4. K.W. Chung and Y.S. Kwon, Jpn.J. Appl.Phys., 27 (1988) L2186.
5. K. Yamaguchi, T. Toyabe, and H. Kodera, J. Appl. Phys. Suppl., 15 (1976) 163.


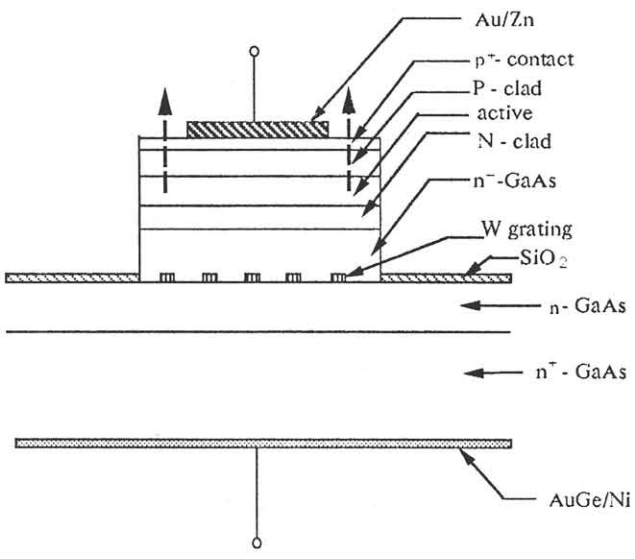


Fig.1. Schematic diagram of the proposed vertical OEIC.

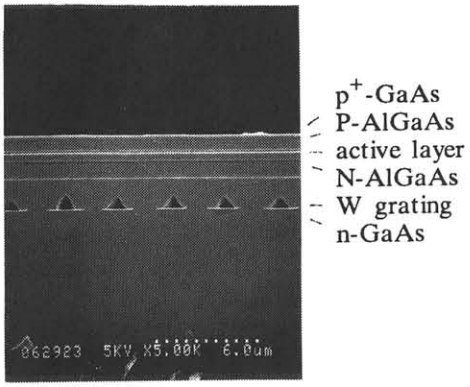


Fig.2. Scanning electron microscope photograph of the overgrown OEIC layer. The triangluar voids are shown on W gratings.

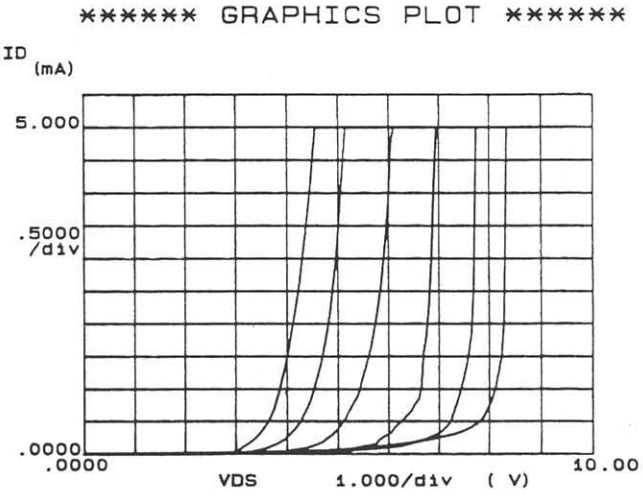


Fig.4. Current-Voltage characteristic of the driver FET in an OEIC.

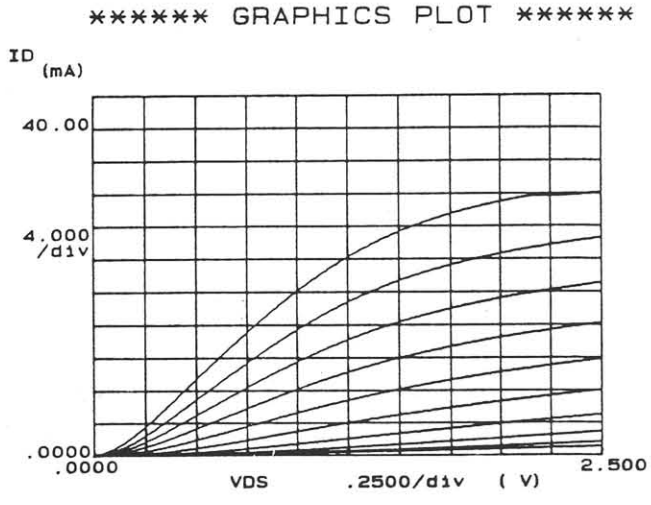


Fig.3. Current-voltage characteristics of the vertical FET. The gate voltage is -0.5V/step from the top curve.

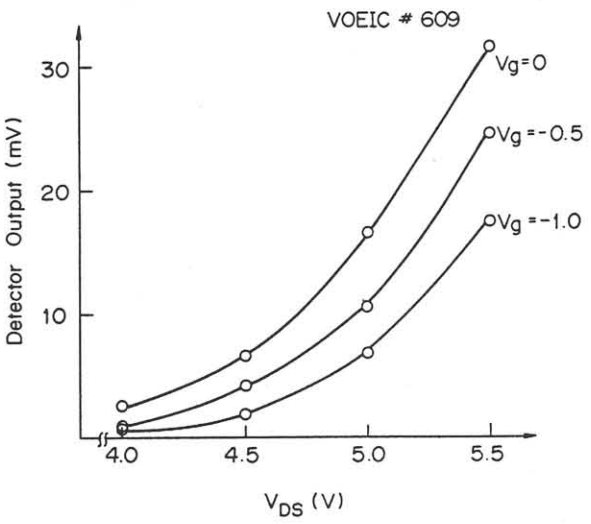


Fig.5. Detector output-$V_{DS}$ characteristic with gate voltage as a parameter.