Extended Abstracts of the 22nd (1990 International) Conference on Solid State Devices and Materials, Sendai, 1990, pp. 649-652

Under Field Oxide Dopant Enhancement (UFDE) for CMOS and BiCMOS Technology

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A structure with dopant enhancement only under field oxide and its implementation are proposed where n-type dopant enhancement is introduced under the field oxide in n-type area of silicon. This technique was applied to 3μm CMOS and BiCMOS technology and it was shown that CMOS and BiCMOS latch-up and collector resistance of the bipolar transistor were improved by adopting this technology. Problems with regards to this technology and possible process optimization are also discussed.

1. Introduction

BiCMOS technology is becoming increasingly important for the realization of VLSI circuit of digital and mixed analog/digital applications[1]. Bipolar device in BiCMOS circuit is required to have low collector resistance (R_C) to increase drivability. To make the bipolar device with low R_C, n^+ buried layer has been employed[2)-4)].

The critical scaling problems in conventional n-well CMOS and BiCMOS technology employed in the n-well CMOS are R_C of bipolar device[5)-6)] and latch-up degradation due to the reduction of n-well to p^+ space and n-well junction depth. Bipolar device with deep n-well(around 7.5μm deep)[6)] has been tried but with little reduction of R_C, and large n-well to p^+ space was required. Also large n-well sheet resistance of scaling n-well CMOS will degrade latch-up immunity of CMOS, especially where guard ring is not allowed due to the density requirement.

In this paper, we introduce a simple structure with n-type dopant enhancement only under the field oxide (hereafter, called UFDE technology) in the n-well region in order to improve the above mentioned characteristics without increasing the n-well junction depth. Resultant CMOS and BiCMOS device characteristics employing UFDE technology will be reported and some of the problems related with the technology will also be discussed.

2. Process Sequence for UFDE Implementation

Simple process sequence to implement the UFDE technology in BiCMOS process merged in conventional n-well CMOS technology has been devised as an example. Starting material is p type <100> silicon wafer with resistivity of 5-7Ωcm. Phosphorus implantation for n-well formation is performed with the dose and energy of 2.5 $\times 10^{12}cm^{-2}$ and 160keV, respectively, and heat cycle is followed. After n-well with sheet resistance of 2.9kΩ/□ and 1.5μm depth is formed, conventional active area is defined. After silicon nitride film is etched, silicon etching step is followed for shallow trench with depth of around 0.3μm (Fig.1 (b)). The shallow trench is introduced to alleviate the degradations of PMOS junction capacitance and the junction breakdown voltage of bipolar and PMOS devices caused by the UFDE structure. After removing the photoresist for active patterning, thin oxide is grown in the shallow trench. The area on p-substrate is protected using n-well mask followed by phosphorus implantation into the shallow trench in n-well to introduce the UFDE region (Fig.1 (c)). Drive-in process for n-well and newly implanted phosphorus under field oxide is performed and

resultant n-well junction depth is about 2.2μm. After field V_T patterning and implantation, conventional field oxide is grown and cross section as Fig.1 (d) is resulted.

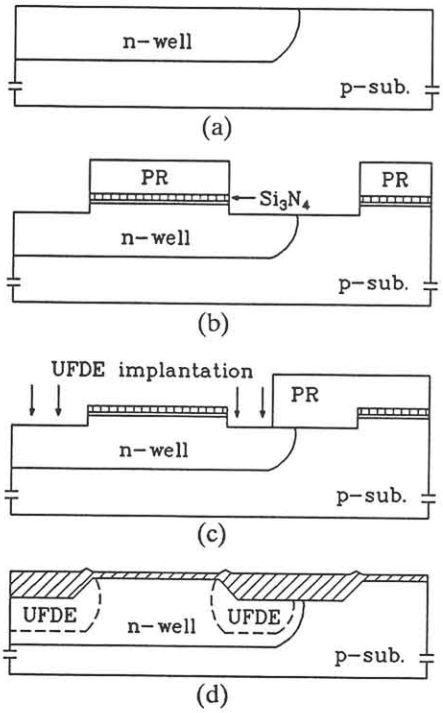


Fig.1 Process sequence for the implementation of UFDE structure.

Once the implementation of UFDE structure is obtained, rest of the process flow for CMOS device is rather conventional. For BiCMOS, we devised simple additional process step to merge the bipolar devices. After the first gate oxidation is grown, boron implantation for base area is performed followed by the oxide strip and the second gate oxide growth with the thickness of 450Å. Emitter area is then opened and gate oxide is wet etched to have the polysilicon emitter area. Then polysilicon film with the thickness of 3200Å is deposited and polysilicon doping by As^+ implantation with the dose of $1\times10^{16}cm^{-2}$ is followed to form the gate area of CMOS device and emitter area of bipolar device. Rest of process is same as CMOS process.

The final structure obtained in our experiment is shown in Fig.2 where collector series resistance components are schematically denoted.

3. Results and Discussion

Vertical doping profile of active bipolar region obtained from the spreading resistance measurement is shown in Fig.3. Emitter junction depth from the polysilicon-silicon interface is 0.1μm and base width is 0.39μm. It should be noted in Fig.3 that collector width and sheet resistance under base are 1.7μm and 5kΩ/□, respectively. Consequently, series resistance component R_1 shown in Fig.2 is expected to be large compared with R_2 and R_3, where R_2 is expected to be reduced by UFDE implantation.

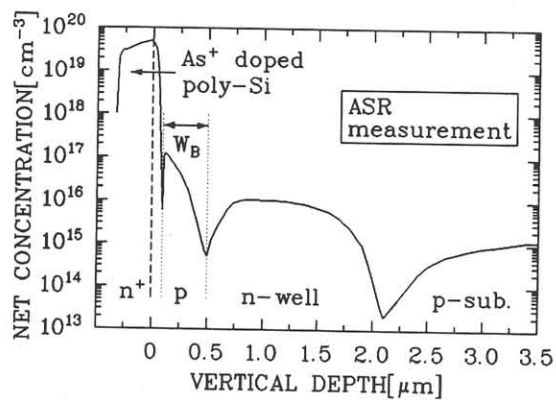


Fig.3 Vertical doping profile of active bipolar region obtained by ASR measurement. As^+ doped polysilicon are used as emitter diffusion source.

Measured sheet resistance of UFDE region is shown in Fig.4 as function of UFDE dose splits. Sheet resistance decreased about 2.5 and 9 times from that of n-well without UFDE implantation and these results means the

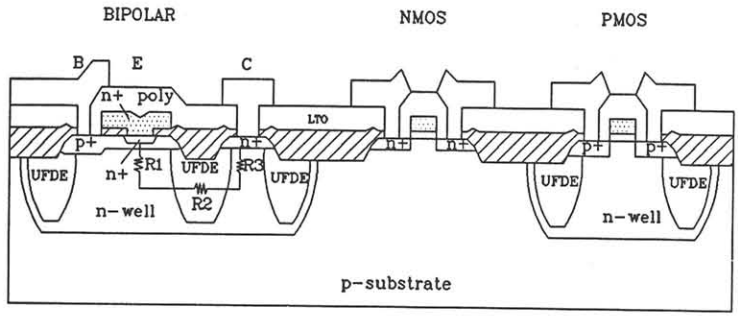


Fig.2 Cross section of fabricated bipolar and CMOS device with UFDE. Equivalent resistance R_1, R_2 and R_3 are shown in bipolar region. R_2 and R_3 are substantantially reduced by the UFDE implantation.

reduction of R_2 shown in Fig.2. Also R_3 as well as R_2 (shown in Fig.2) can be reduced by UFDE insertion.

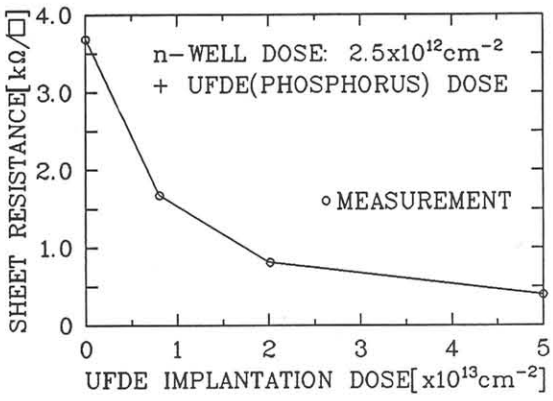
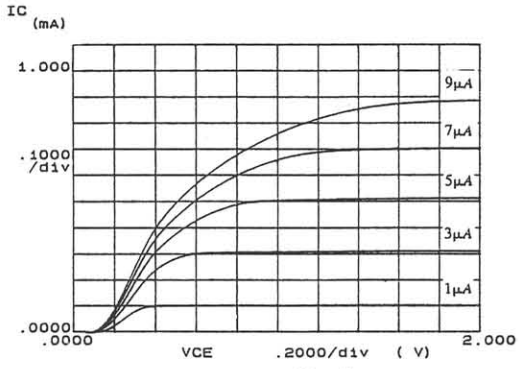


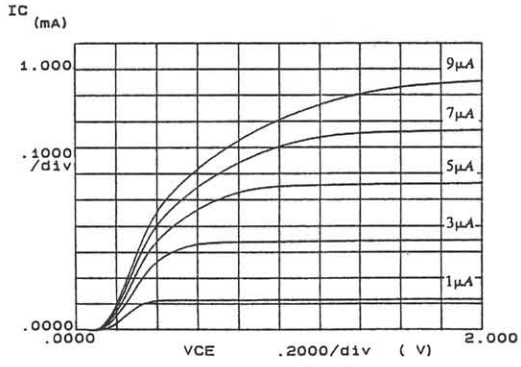
Fig.4 Sheet resistance versus UFDE doses for the n-well under the field oxide.

Fig.5 (a), (b) and (c) show I-V characteristics of bipolar devices with three UFDE doses of 8×10^{12}, 2×10^{13} and $5\times10^{13}cm^{-2}$, respectively. Improvement in total collector resistance with UFDE dose increase is obviously observed and collector resistances for each device are 500Ω(a), 450 Ω(b) and 390Ω(c), respectively. Considering large series resistance R_1 due to the large n-well resistance (shown in Fig.2), the effect of R_2 reduction on total collector resistance is quite significant.

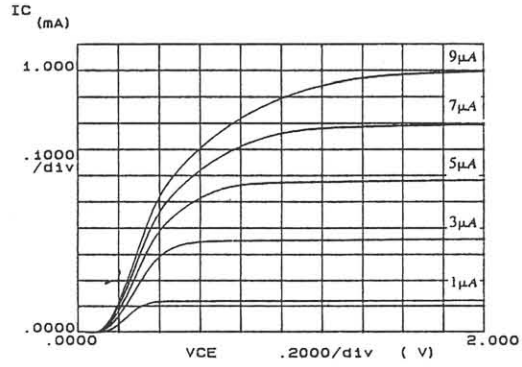
Fig.6 shows the holding current of V_{CC}-V_{SS} latch-up characteristics for 19-stage CMOS and BiCMOS ring oscillators. In this figure, data for conventional CMOS with n-well depth of 4μm and R_S of 2.5kΩ/□ are shown as a reference. It can be seen that CMOS devices with UFDE implantation show better latch-up characteristics than that of conventional CMOS device. These phenomena can be explained by the guard ring effect of UFDE region (self aligned guard-ring under the field oxide) and reduced n-well lateral diffusion. Weak latch-up characteristics by shallow n-well depth was compensated by UFDE guard ring effect and reduced lateral diffusion of n-well. The decrease of latch-up immunity with UFDE dose increase can be understood by the degradation of PMOS source-drain junction breakdown. BiCMOS latch-up immuntiy is increased with UFDE dose since collector resistance of bipolar device and parasitic resistance in latch-up triggering path are reduced by the UFDE insertion. In case of BiCMOS



(a) $8\times10^{12}cm^{-2}$



(b) $2\times10^{13}cm^{-2}$



(c) $5\times10^{13}cm^{-2}$

Fig.5 Collector current versus collector-emitter bias for the devices (emitter area: $3\times6\mu m^2$) with three different UFDE implantation doses of (a) 8×10^{12} cm^{-2}, (b) $2\times10^{13}cm^{-2}$ and (c) $5\times10^{13}cm^{-2}$.

circuit with PMOS and bipolar devices in the same n-well, parasitic resistance reduction under the field oxide due to the UFDE has positive effects on latch-up characteristics as well as collector resistance reduction of bipolar device.

One of the problems with implementation of UFDE technology is expected in the degradation of bipolar base-collector and PMOS drain junction breakdown voltage as can be seen in Fig.7 where several breakdown voltages

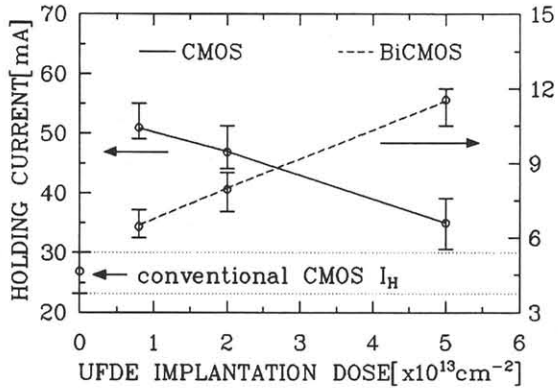


Fig.6 Holding current (I_H) of latch-up characteristics of CMOS and BiCMOS ring oscillators with UFDE dose variations.

of bipolar devices are shown against UFDE doses. It can be seen that BV_{CEO} decreases as UFDE dose increases. Notable point in Fig.6 is that BV_{CEO} is larger than BV_{CBO}. This phenomenon can be understood by the fact that collector-base breakdown takes place in the base-collector junction perimeter butted to the field oxide so that BV_{CEO} of bipolar transistor is relatively irrelevant to BV_{CBO} of vertical bipolar transistor.

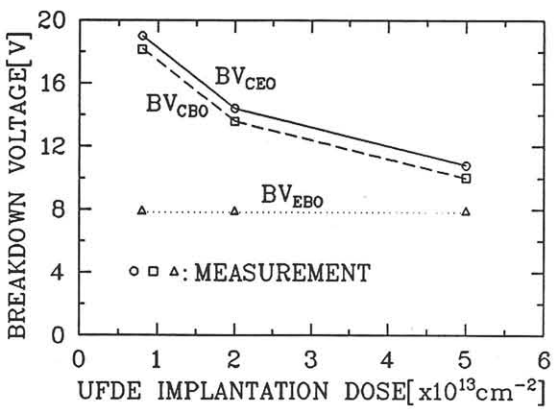


Fig.7 Breakdown characteristics of bipolar transistor with UFDE variations.

Fig.8 shows the narrow channel effect of PMOS due to phosphorus lateral diffusion of UFDE region. PMOS threshold voltage increase with the decrease of channel width is substantial especially for the device of high UFDE dose. Improvement of the junction breakdown voltage and the narrow channel effect of the PMOS device can be achieved by the UFDE process optimizations, one of which may be the deeper silicon etch on the field area than employed in this experiment and formation of oxide side-wall around the trench before UFDE implantation.

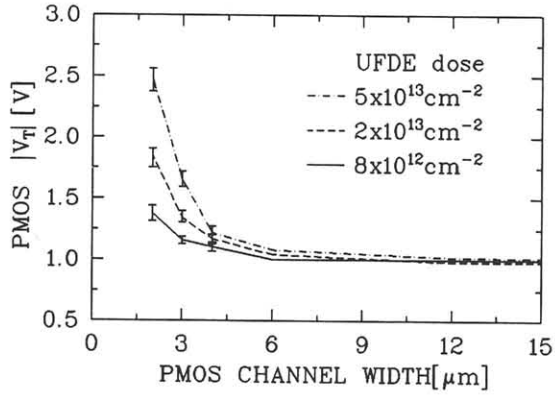


Fig.8 PMOS threshold voltage variations versus PMOS channel width with UFDE doses as parameters.

4. Conclusions

We have proposed a structure with n-type dopant enhancement only under field oxide in n-well of CMOS together with simple process sequence to implement it. Bipolar and CMOS devices with the proposed structure were fabricated and characterized. The collector resistance of bipolar transistor was improved due to the reduction of n-well resistance under the field oxide. Improvement in latch-up characteristics of the BiCMOS and CMOS circuits were found and compared with the conventional CMOS devices. Several problems occured with the UFDE structure and possible process optimization were also discussed.

Acknowledgements

The authors would like to thank the process engineers of Inter-university Semiconductor Research Center for their experimental supports. Also it should be addressed that parts of device fabrication were performed at Samsung Electronics Corporation and Gold-Star Electron Corporation.

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