

A 3.8 ns, 800 mW 256 K Bipolar SRAM

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An ECL-compatible 32k x 8 bipolar SRAM that features a nominal access time of 3.8 ns at 600/800 mW standby/select power and a packing density of > 5k bit/square mm has been designed in a standard bipolar technology. The chip is being fabricated in a process using 1 μ m dimensions, double-polysilicon self-aligned transistors, and trench isolation. Early test site hardware has fully verified the memory cell concept.

INTRODUCTION

For very-high-speed SRAM applications like cache and control store in mainframe computers, the bipolar technology offers a speed advantage over CMOS and BICMOS. The fast bipolar SRAMs often utilize SCR-type memory cells^(1,2) that allow a short access time, but their density and power dissipation are not as attractive. On the other hand, I²L/MTL memory products have proven to eliminate these drawbacks, but some read performance has been traded off⁽³⁾.

This paper describes the design of an ECL-compatible 32k x 8 MTL/I²L SRAM that features a typical access time of 3.8 ns at a power dissipation of only 600 mW in standby and 800 mW in select mode. The chip is being fabricated in a standard 1 μ m bipolar technology with double-polysilicon self-aligned transistors of $f_T = 16$ GHz and trench isolation (photomicrograph before final metal in Fig.1). The main characteristics of this first 256k bipolar SRAM are

summarized in Figure 2. Early test site hardware has been analyzed that have fully verified the memory array concept.

MEMORY CELL

Key for the high density and excellent speed/power of the SRAM is the Split-Emitter MTL memory cell⁽⁴⁾ in Figure 3, which has been derived from the Injector Sensed (IS)⁽³⁾ cell used in earlier SRAM products. The common emitters of the IS cell have been separated, and the two cell halves are coupled via booster resistors R1 and R2 to the word-address line. As a result, the sense signal at the bit lines B0 and B1 is increased by the voltage difference across the resistors, significantly enhancing the read access. The schematic cell cross-section and layout illustrate that the basic cell utilizes two cross-coupled MTL inverters. The booster resistors are implemented by P-polysilicon resistors and are shared by 4 cells, thus limiting its area consumption to < 10% per cell.

ARRAY ARCHITECTURE

As can be recognized from the chip photomicrograph in Fig.1, the total memory cell array is divided into 32 subarrays (macros) of 8k cells. By this measure, only one array macro is powered up during chip select thus considerably enhancing the power/performance.

Each word line WL in a macro requires only one transistor for the word drive switch and one diode for the standby current supply. Therefore, the additional area for word peripherals due to the distributed word line scheme is negligible. The schematics for the word circuitry are shown in more detail in Figure 4. The single-level decoding is performed by means of charge storage diode AND circuits that are controlled by high-current push-pull ECL address phase splitters providing large dynamic currents. This measure significantly saves DC power without sacrificing speed.

The bit circuitry is more complex because of the shared booster resistors and the relatively slow cell performance due to the lateral cell PNP transistors. Figure 5 shows the bit line switches required to perform a fast read or write operation. The timing control of the switches gated by the macro decoder is crucial for the read access time. Because of the relatively small read signal at the bit lines, a multistage preamplifier with few output dots at the first stage has been utilized. Figure 6 shows the simulated waveforms of the key signals for the read operation at a worst-case bit pattern. The nominal access time is 3.8 ns from chip select or clock input to data output.

EXPERIMENTAL CELL RESULTS

Experimental results from early test site hardware (Fig.7a) have confirmed the memory cell characteristics and operating conditions. Almost ideal current voltage characteristics have been measured even far below the cell standby current of 10 nA (Fig.7b), as shown by the Gummel plots of the PNP and inverse NPN transistors of the MTL cell in Figures 7b and 7c, respectively. The current gain of the inverse cell NPN (merged with a PNP) is much higher than the minimum value of > 1 that is required to assure cell stability.

CONCLUSIONS

This 256 k SRAM design with a nominal access time of 3.8 ns at only 600 mW/800 mW standby/select power has demonstrated that high-density SRAMs with excellent speed/power are feasible in standard bipolar logic processes. As a result, relatively large SRAMs as required for caches and control stores can be implemented with fairly large logic circuitry on the same chip for optimum system performance.

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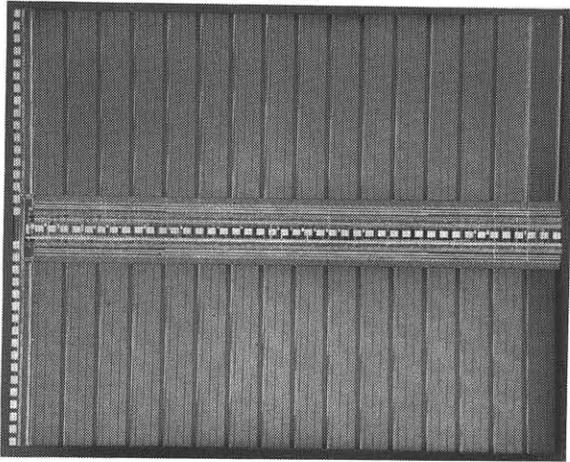


Fig.1: Photomicrograph of 256k MTL SRAM

Technology : 1 um, Double-Polysilicon
Self-Aligned Transistors,
Trench Isolation

Organization : 32K x 8

Memory Cell : MTL Split-Emitter Cell

Cell Size : 134 square um

Chip Size : 7.9 x 6.3 = 49.8 square mm

Access Time (nom) : 3.8 ns

Cycle Time (nom) : 12 ns

Power (STB/SEL.) : 600 / 800 mW

Interface : ECL (+ 500 mV)

Power Supplies : (+1.4 V, -0.7 V, -2.2 V)

Fig.2: Key SRAM Characteristics

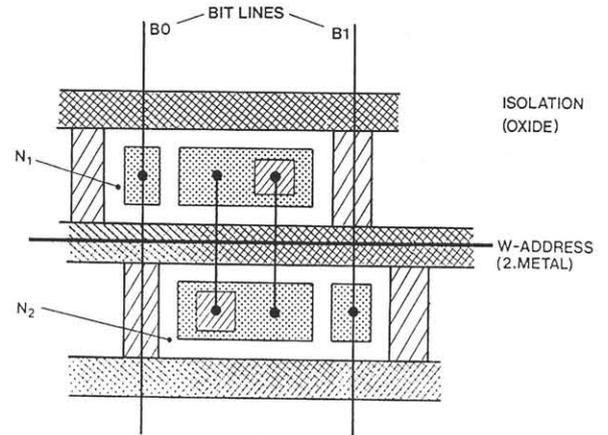
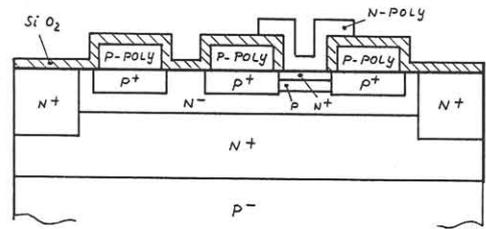
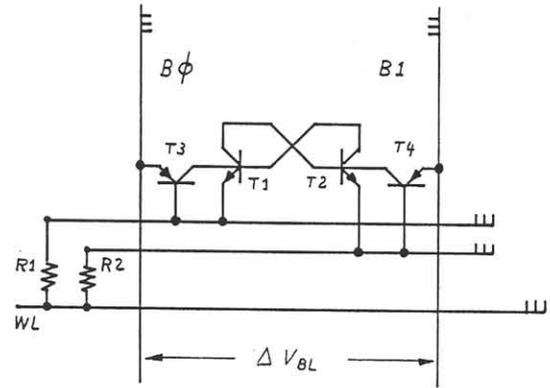


Fig.3: Split-Emitter MTL Cell

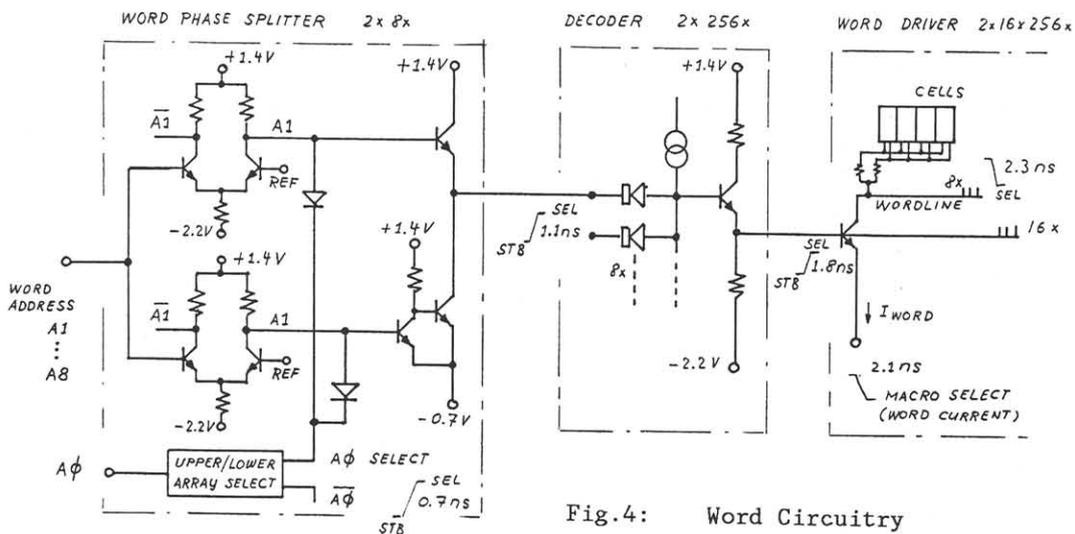


Fig.4: Word Circuitry

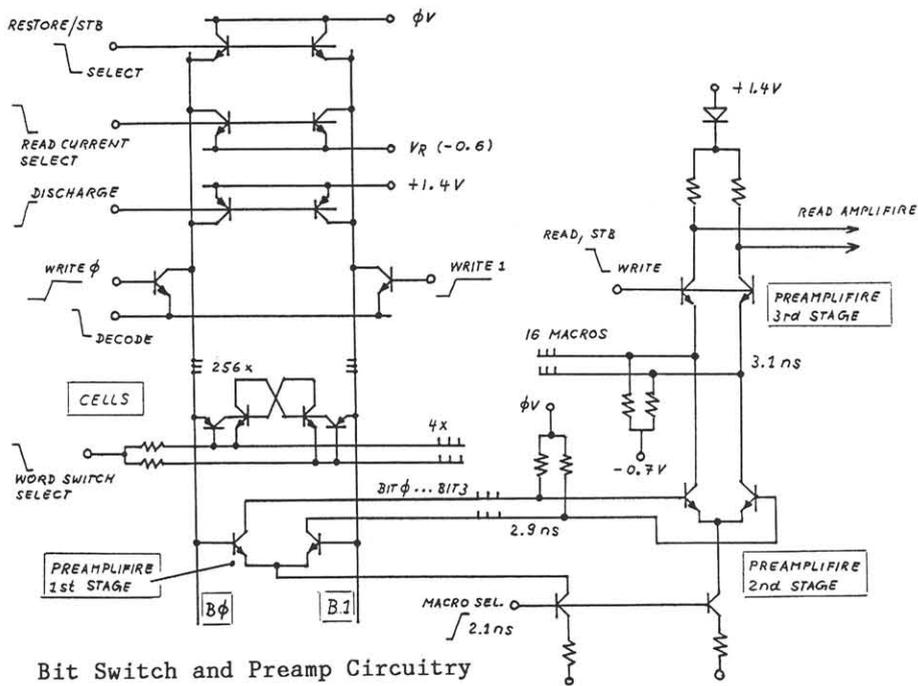


Fig.5: Bit Switch and Preamp Circuitry

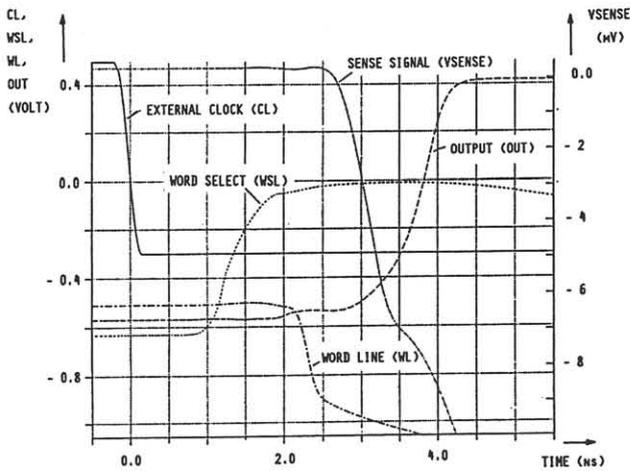


Fig.6: Waveforms for Read Access

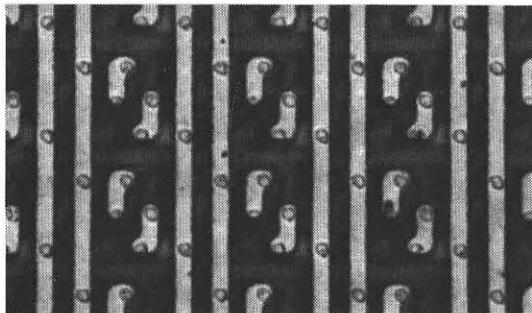


Fig.7: Memory Cell Experiments

- a) Photomicrograph of Memory Cell
- b) Measured Current / Voltage Characteristics of Inverse NPN
- c) Measured PNP Characteristics

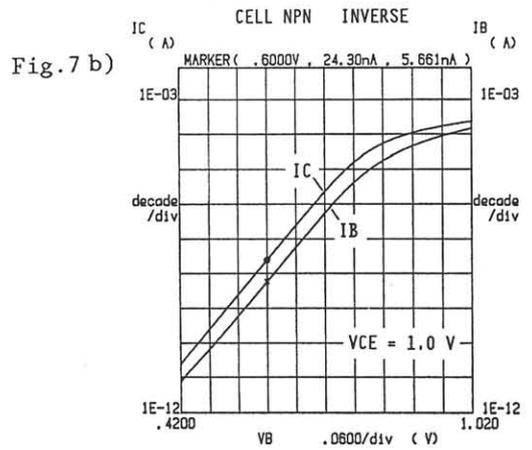


Fig.7 b)

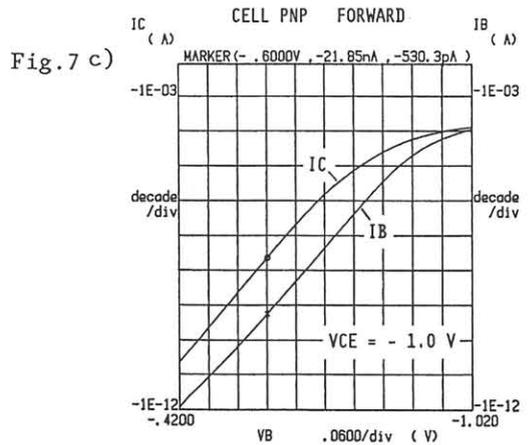


Fig.7 c)