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Selective Polysilicon Deposition (SPD) by Hot-Wall LPCVD and Its Application to High Speed Bipolar Devices

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Selective polysilicon deposition (SPD) is achieved on Si_3N_4-patterned substrate using a $SiH_2Cl_2/HCl/H_2$ gas system in a hot-wall LPCVD reactor. Sufficient selectivity and growth rate are obtained at a suitable HCl mole fraction, which depends on growth temperature and total pressure. This SPD technology is successfully applied to shallow emitter formation of high speed bipolar devices, resulting in the remarkable reduction of the emitter resistance.

INTRODUCTION

Contact filling technology has become very important in the ULSI device fabrication. Recently, considerable attention has been paid to selective polysilicon deposition (SPD) for self-aligned contact filling and shallow junction formation. Depositions were typically carried out using a SiH_2Cl_2/H_2 or $SiH_2Cl_2/HCl/H_2$ gas system in a cold-wall LPCVD reactor [1][2]. SPD based on Si_2H_6 decomposition was also reported [3]. In all the previous reports, SPD was studied on SiO_2-patterned substrates. In this study, SPD has been examined on Si_3N_4-patterned substrates using a $SiH_2Cl_2/HCl/H_2$ gas system in a hot-wall LPCVD reactor. It is more difficult to obtain sufficient selectivity on Si_3N_4 windows than SiO_2 ones, since silicon nucleation tends to take place more easily on Si_3N_4 films than SiO_2 [4][5]. The optimized SPD was applied to the self-aligned shallow emitter formation of the high speed bipolar devices, which was fabricated using Advanced BSA (BSG Self-Aligned) technology [6].

EXPERIMENTAL

The reactor is a conventional vertical hot-wall type, utilizing a resistance-heated furnace. Substrates were charged in a stack on a rotating substrate holder. The $SiH_2Cl_2/HCl/H_2$ mixture was introduced via a gas distributor and injected into the substrate spacing. A schematic cross-sectional structure of prepared samples is shown in Fig. 1. Prior to SPD, the substrates were dipped in diluted HF. Then they were prebaked in situ in H_2 at growth temperatures. All the experiments were carried out at a fixed SiH_2Cl_2 flow rate of 300 sccm. The growth temperatures varied between 750 and 850 °C and the total pressure varied between 15 and 30 torr. Selectivity was investigated by dark-field optical microscopy. The measurement of the film

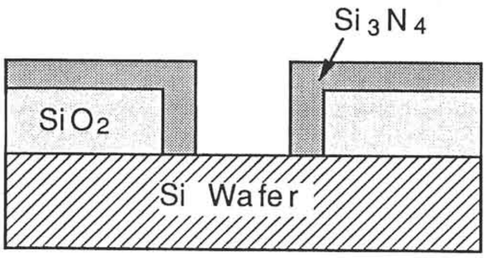

Fig. 1 Schematic cross-section of the Si_3N_4 window.

thickness and the observation of the film quality were performed using SEM and TEM techniques.

The schematic cross-sectional structure of the Advanced BSA transistor, to which this SPD film was applied is shown in Fig. 2 [6]. The buried emitter electrode consists of As^+-implanted SPD film, PtSi and selectively deposited W layers.

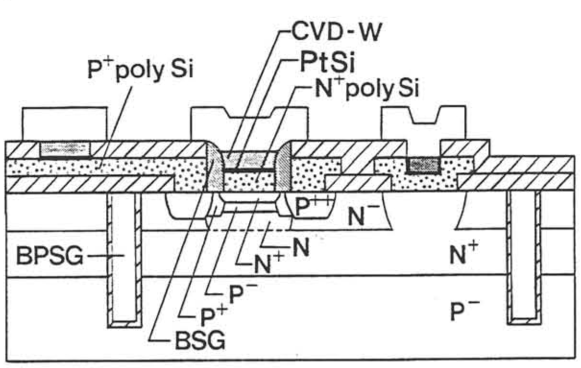

Fig. 2 Schematic cross-section of the Advanced BSA transistor.

RESULTS and DISCUSSION

1. Selective Polysilicon Deposition

The growth rate is shown in Fig. 3 as a function of HCl flow rate for different temperatures. The HCl flow rate exerts a profound influence on selectivity and growth rate for each temperature. Decreasing HCl flow rate causes non-selective deposition and larger growth rate. On the other hand, increasing HCl flow rate leads to decrease in the growth rate and enhances selectivity. The polysilicon deposition with sufficient selectivity is obtained in the limited HCl flow rate range. The growth rate decreases linearly on a semilog scale with the HCl flow rate. The slope is almost independent of temperatures in the range of 750 to 800 °C. This indicates that the HCl flow control is very important to obtain stable SPD .

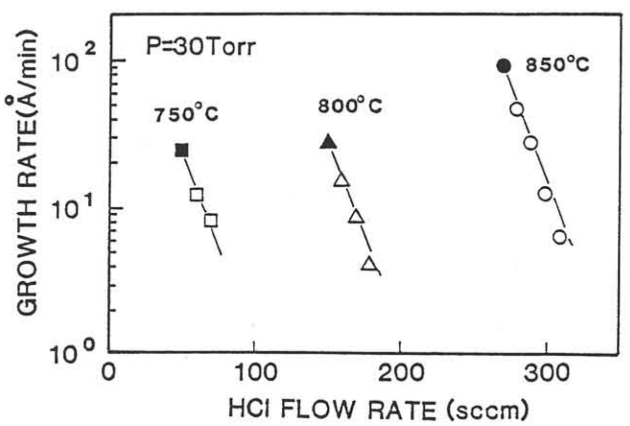

Fig. 3 Growth rate as a function of HCl flow rate for different temperatures.
□ △ ○ : Selective
■ ▲ ● : Non-selective

The selectivity can be enhanced by the growth temperature elevation. In order to maintain sufficient selectivity, however, the temperature elevation has to be accompanied by the increase in the HCl flow rate. This is attributed to silicon nucleation enhancement on Si_3N_4 with increasing growth temperature in the $SiH_2Cl_2/HCl/H_2$ gas system [5].

Figure 4 shows the growth rate dependence on HCl flow rate for different pressures. The higher pressure requires an increase in the HCl flow rate to maintain sufficient selectivity. The growth rate of selective deposition increases with increasing total pressure.

SEM images of polysilicon films deposited at various temperatures are shown in Fig. 5. A smooth surface is obtained at the low temperature

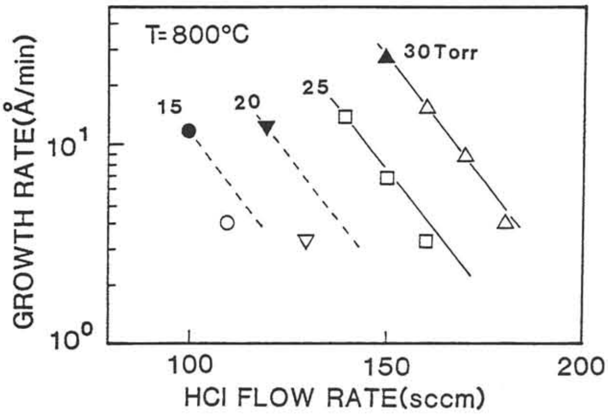

Fig. 4 Growth rate as a function of HCl flow rate for different pressures.
○▽□△ : Selective
●▼ ▲ : Non-selective

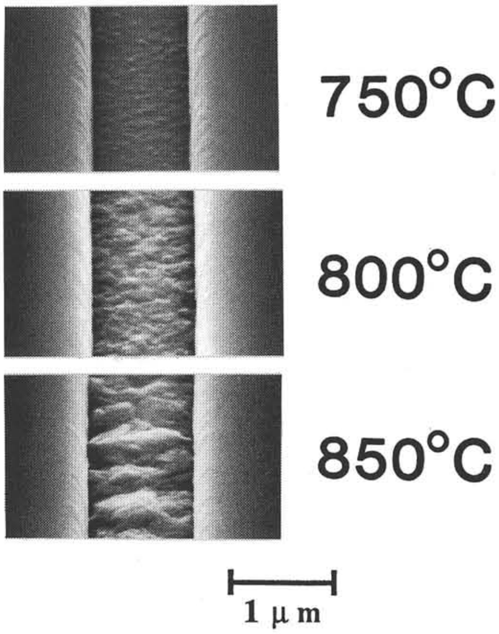

Fig. 5 SEM images of the polysilicon film deposited at 30 torr.

deposition. However, at the high temperature the surface becomes rough due to the grain growth. The polysilicon film deposited at 800 °C was observed by cross-sectional TEM as shown in Fig. 6. The polysilicon film consists of grains with high twin density. Figure 7 shows that the growth rate is almost independent of window size in the range of one hundred to the submicron squares. This indicates that the polysilicon deposition is limited by the surface reaction. From a view point of applying to the fabrication of devices with various patterned sizes, this is a very useful result.

2. Application to bipolar devices

SPD was applied to the Advanced BSA transistor fabrication. As shown in Fig. 8, 1500Å thick polysilicon with smooth surface morphology was selectively deposited at 800 °C and 30 torr on the emitter contact, whose size and aspect ratio are 0.4 μm^2 and 1.5, respectively. As^+ ion implantaion was carried out at 70 KeV to doses of $1 \times 10^{16} cm^{-2}$. The device parameters of this Advanced BSA transistor are shown in Table 1. This emitter structure, having PtSi and CVD-W on the SPD film reduces the emitter

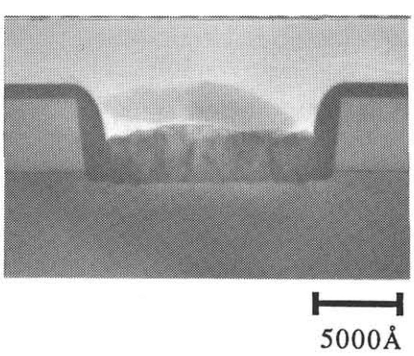

Fig. 6 Cross-sectional TEM image of the 3000Å thick SPD film on a Si_3N_4 window.

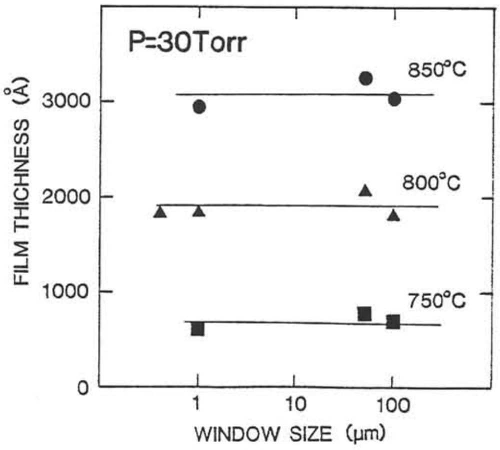

Fig. 7 SPD film thickness as a function of window size.

resistance to 1/4 that of a conventional structure because of the extinction of the emitter polysilicon refilling effect [7]. The high device performances of cut-off frequency f_T of 40 GHz at V_{CE} of 1V and h_{FE} of 50 are obtained.

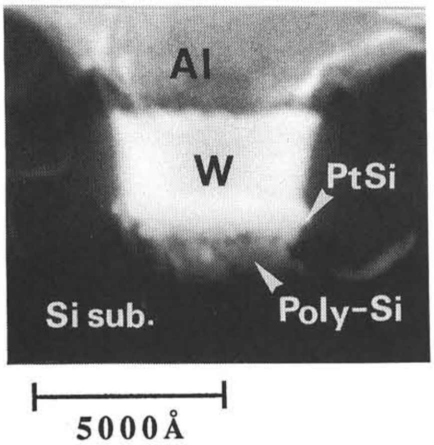

Fig. 8 Cross-sectional SEM image of the buried emitter electrode structure.

DEVICE PARAMETERS

Emitter area	S_E (μm²)	0.4x0.4
Collector-base capacitance	Cjc(fF)	3.1
Collector-substrate capacitance	Cjs(fF)	6.3
Emitter resistance	R_E (Ω)	110
Base resistance	R_B (Ω)	450
C-E breakdown voltage	BV_{CEO}(V)	2.7
E-B breakdown voltage	BV_{EBO}(V)	2.0
Current gain	h_{FE}	50
Maximum cut-off frequency	f_T (GHz)	40

Table 1 Device parameters of the Advanced BSA transistor.

CONCLUSION

SPD with smooth surface morphology has been successfully achieved on submicron sized Si_3N_4 windows using a $SiH_2Cl_2/HCl/H_2$ gas system. Sufficient selectivity is obtained at a suitable HCl mole fraction, which depends on growth temperature and total pressure. The first application was performed to high speed bipolar devices. The advantage of this technology was demonstrated by the drastic reduction of the emitter resistance. This SPD technology is promising for self-aligned contact filling in future ULSI fabrication.

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