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SOA Improvement of p-Channel IGBT

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A p-channel IGBT, which is supposed to be useful for inverter application, has been developed. SOA in the p-channel IGBT is not limited by latch-up as in the case of a n-channel IGBT, but limited by electron avalanche multiplication, which triggers a catastrophic carrier increase in high electric field. It is demonstrated that utilizing high resistivity (over 300Ωcm) p-base is effective to suppress peak of electric field and improve SOA without a substantial increase of on-state voltage drop.

1. Introduction

The Insulated Gate Bipolar Transistor (IGBT) has been extensively developed because of its high performance with low on-state voltage drop(V_{on}) and high input impedance[1),2)]. Much efforts were devoted for the n-channel IGBT so far, because this device has many applications such as n-channel power MOSFET and npn bipolar transistor[3)]. However, it is supposed that the p-channel IGBT (Fig.1) can supply new circuit applications such as inverter application and freedom for circuits designers.

However, some researchers pointed out that p-channel IGBT has smaller safe operating area (SOA) than n-channel one because of its wide base npn structure [4),5),6),7)].

In this report, we clarify turn-off failure mechanisms of the p-channel IGBT by numerical simulation and show possibility for improvement of SOA from results of trial fabrications.

2. Safe Operating Area(SOA) of IGBT

SOA is defined as capability of turn-off area of current and voltage without any failure. In usual power semiconductor switches lowest current limit is set at double of its typical current with 80% of static blocking voltage. For instance, 600V/50A device is required to cut off current of 100A at 500V without any destructive switching within whole operative temperature region. SOA of IGBT is restricted by two different phenomena. One is so called latch-up, which is due to its parasitic thyristor. The other is avalanche multiplication at high electron current density, which plays an important role in the case of the p-channel IGBT. We discuss the latter mechanism in the following.

Maximum electric field at p-base is roughly estimated by the following equation[7)]

$$E_{max}=2q\cdot V_{CE}\cdot(N_{sub}+J_c/e\cdot v_{sat})^{1/2}/\varepsilon_{Si}, \quad (1)$$

where V_{CE} is applied voltage, N_{sub} is impurity concentration of p-base, v_{sat} is saturation velocity of electron, and ε_{Si}

is dielectric constant of silicon. As easily seen from Eq.(1), E_{max} increases as J_c and N_{sub} increase. On the other hand avalanche multiplication factor caused by ionization impact is strongly dependent on the electric field and the type of carrier. Under the same electric field, multiplication factor of electron is several orders of magnitude larger than that of hole. The electrons added by this multiplication work as the base current of the wide-base npn transistor. This process acts as positive feedback to induce latch-up, which happens rather easily in the p-channel IGBT than in the n-channel IGBT.

Though several approaches were proposed so far[8),9),10)] to prevent latch-up for n-channel IGBT (for example deep p^+ well to reduce the base-short resistance of parasitic thyristor), they are not necessarily effective for p-channel IGBT. This fact strictly restricts the width of our selection to improve SOA. The p-channel IGBT has been considered as a difficult device to control[5),6)].

3. Simulation

Turn-off characteristics are analyzed by 2-dimensional dynamical simulator for bipolar devices (FBIDES)[11)]. If any kinds of breakdown process are expected in the device, electron-hole pair recombination and creation by avalanche multiplication should be included in the simulation correctly. These terms are taken into consideration in the current continuity relations as follows

$$\partial p/\partial t=-\mathrm{div}J_p/e+G-U, \quad (2)$$

$$\partial n/\partial t=\mathrm{div}J_n/e+G-U, \quad (3)$$

$$G=(\alpha_p \cdot J_p+\alpha_n \cdot J_n)/e, \quad (4)$$

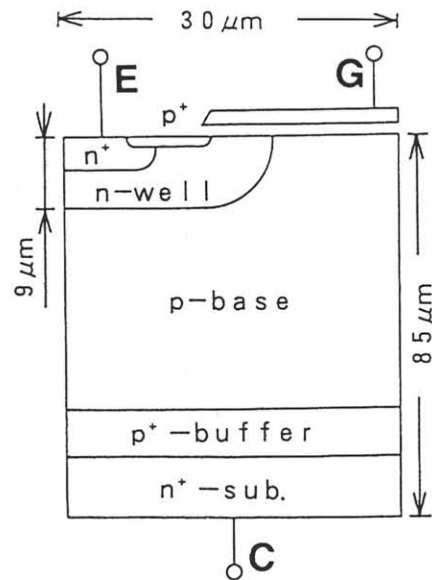

Fig.1 structure of the p-channel IGBT and dimension of simulated device.

$$\alpha_{p,n}=A_{p,n}\cdot \exp[-(b_{p,n}/E)^m], \quad (5)$$

where p and n are hole and electron density respectively, G is carrier generation rate, U is carrier recombination rate, J_p and J_n are hole and electron current density respectively, and E is electric field.

Dimension of simulated device configuration is shown in Fig.1. Numerical analysis is carried out for various value of p-base specific resistivity, ρ_p, and buffer layer width, w_b.

Fig.2 shows capable turn-off voltage V_{sus}, at current density of $188A/cm^2$, which corresponds to current of 100A for $8.2x8.2mm^2$ chip. First, high specific resistivity can improve V_{sus} about 30-40% compared with the value at 100Ωcm as expected from Eq.(1). Current density of $188A/cm^2$ corresponds to charge density of $10^{14}cm^{-3}$, assuming that all current is due to electron and $v_{sat}=10^7cm/s$. This figure corresponds to p-base acceptor concentration at about 130Ωcm. V_{sus} saturates at the range of over 500Ωcm.

This can be interpreted that V_{sus} is limited by electron current charge rather than acceptor charge in the depletion region of p-base at over 500Ω cm, that is

$$N_{sub} \ll J_c/e \cdot v_{sat} \qquad (6)$$

Secondly, the wider the p-buffer is, the higher V_{sus} is. Wider buffer width reduces h_{fe} of wide-base npn transistor and positive feedback is hardly occurred. It should be noted that wider buffer layer may increase on-resistivity because minority carrier injection ratio from anode-region is restrained.

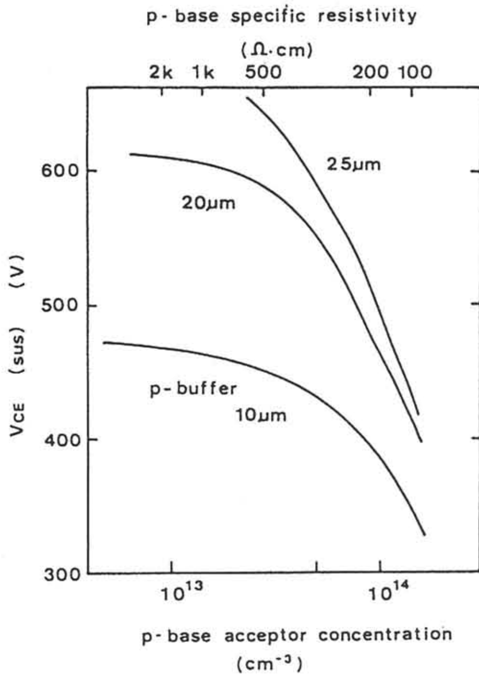

Fig.2 Capable turn-off voltage at 188A/cm^2 for various buffer-width.

4. Experimental results and discussion

8.2x8.2mm^2 p-channel IGBT is fabricated. Wafers of various specific resistivity of p-base are grown by epitaxial method on (100) n-type substrate. p-base epitaxial layer width is 55μm. Conductive polarity of ultra high resistivity of 6000Ω cm is assured by the existence of p-n junction. Long stripe cell pattern is adopted. Wafer process is normal MOS process. Electron irradiation with high energy is introduced to control switching speed.

p-base resistivity is ranged from 75 Ω cm to 6000Ω cm. Results of SOA are shown in Fig.3, where all dotted points are safe points. Obviously SOA has been improved for higher p-base resistivity, although saturation of SOA improvement is seen as expected from simulation.

Temperature dependence of SOA is presented in Fig.4. SOA is a little bit wider in high temperature(150℃) than in R.T. This difference of temperature dependence from the n-channel IGBT is caused by the different mechanism of destructive failure in this device. At higher temperature avalanche multiplication is restrained by the frequent collision with phonons, while p-well resistivity becomes higher and latch-up easily happens in the n-channel IGBT.

High resistivity of p-base does not always mean high on-resistance because of conductivity modulation in p-base at on-stage. Fig.5 shows the resistivity dependence of V_{on}. For a comparison, the same

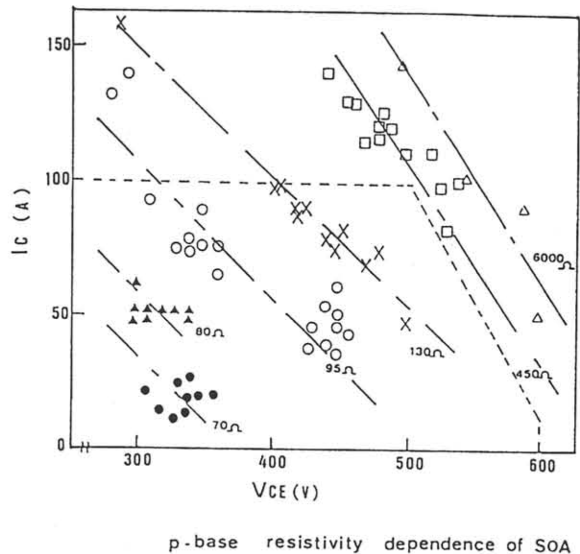

Fig.3 SOA of 8.2x8.2mm^2 chip at R.T.

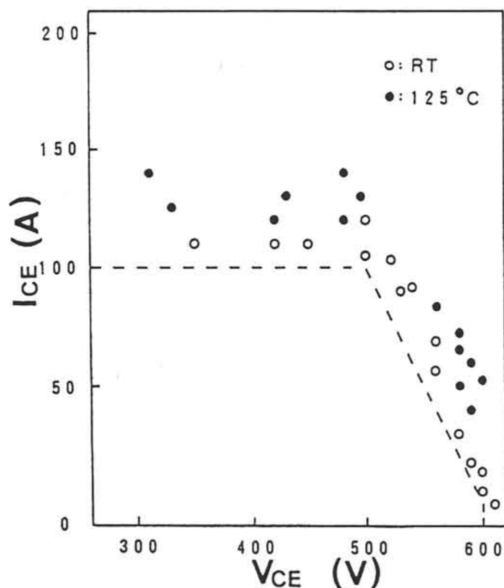

Fig.4 Temperature dependence of SOA.

turn-off speed (around 0.75µs) is taken. V_{on} becomes slightly higher as p-base resistivity increases. It is well known that JFET effect becomes important in the high resistivity region in power-MOSFET[12]. Thus, the result of Fig.5 is explained by JFET effect. However, this effect is not so serious in IGBT because of conductivity modulation.

5. Conclusions

Numerical and experimental studies on the SOA of p-channel IGBTs were presented. The failure mechanism of p-channel IGBTs during turn-off was clarified and a way to improve the SOA is proposed and verified experimentally.

(1) The turn-off failure in p-channel IGBT occurs when avalanche current turns on the base-current of wide-base npn transistor in the IGBT.

(2) The SOA improvement is achieved by using the high resistivity p-base of over 300Ω cm without serious increase of V_{on}.

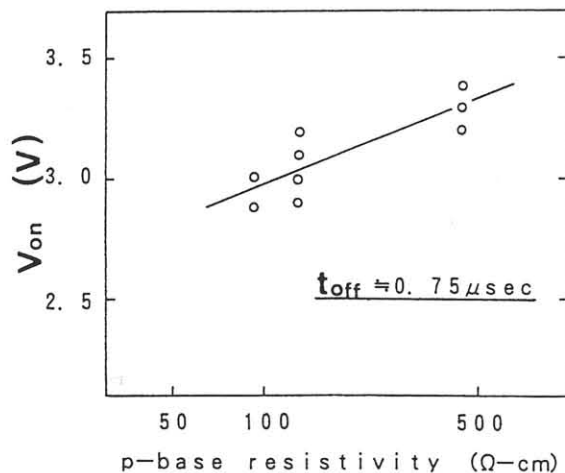

Fig.5 V_{on} at various p-base resistivity.

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