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1/2″ 600 k-Pixel Interline Transfer CCD Image Sensor with Single Poly-Silicon Electrode Structure

Kumio GUNDO, yoshiyuki MATSUNAGA, and Nozomu HARADA

TOSHIBA ULSI Research Center
1.Komukai Toshiba-cho, Saiwai-ku, Kawasaki, 210, Japan
phone:044-511-2111

A 1/2 600k-pixel interline transfer CCD imager with single poly-silicon layer structure has been proposed and fabricated. The new CCD structure gives a three times larger signal charge handling capacity than the conventional double poly-silicon layer electrode structure at 1.2μm channel width. This device has realized high resolution and wide dynamic range.

1. INTRODUCTION

A resolution improvement is challenging for CCD Image sensors, and require shrinking the pixel size 1),2). Shrinking the pixel size leads to a reduction in signal charge handling capability, resulting in dynamic range decrease. Therefore, a pixel structure with large charge handling capability is required for the high resolution CCD. A few development efforts have been reported so far with reasonable resolution. However, none of them is applicable for practical use in a video camera with respect to fabrication process difficulties. The authors have realized a 1/2" 600k-pixel CCD with a large charge handling capability of 4×10^4 electrons by using a single poly-silicon layer electrode structure for the CCD register. The fablication process is much simpler than the conventional fabrication process.

2. SINGLE LAYER ELECTRODE CCD

Figures 1 (a) and (b) show cross section SEM photographs of a conventional double poly-silicon CCD and a new single poly-silicon CCD, respectively. The transfer electrodes are arranged close to neighboring electrodes. The spaces between the electrodes generate potential pockets in the transfer channel under them, resulting in transfer efficiency degradation. The double layer structure was invented in order to make the spaces narrower and to suppress the pocket. At present, a buried channel CCD with this double layer structure achieves complete transfer under suitable driving conditions. The complete transfer CCD is an ideal device with no additional noise. On the contrary, the double layer structure has a serious problem caused by the oxide quality in the space section. The problem involves the low breakdown voltage between the first poly-silicon layer and the second layer, which makes CCD scale reduction impossible. This is because the inter poly-silicon oxide layer is a compound oxide made from poly-silicon

and from the substrate. The difference in the oxide growth rates between poly-silicon and the substrate results in the substrate stress. This causes surface leak current. As mentioned above, the double poly-silicon structure, which improved the CCD performance dramatically, causes several degradations. On the other hand, the single layer structure has no problem involving inter poly-silicon oxide layer breakdown. The potential pocket under the space was analysed with the two dimensional device simulation. Figure 2 shows the simulated results. The narrower space generates a smaller pocket. In the region under 0.5μm space, the pocket is not observed under 5V driving condition. Figures 3 (a) and (b) show a cross-sectional view of a wide space single layer CCD and the channel potential simulation results. The channel potential under the space could be controlled by applying DC voltage to the aluminum optical shield. Figure 4 shows the experimental results of transfer efficiency for 1.2μm space single layer electrode structure CCD. The transfer efficiency could be improved by applying -21V DC to the aluminum optical shield.

3 IMAGE CELL

Figures 5 (a) and (b) show stain-etched cell patterns for a conventional CCD cell and for the new single layer CCD cell. The channel stop region under the second poly-silicon layer, is wider than that under the first poly-silicon layer, because of lateral diffusion by second gate oxidation. Therefore, the buried channel region becomes narrower, resulting in smaller handling capability. On the other hand, the channel stop region is narrower and the the buried channel is wider in the new CCD cell, resulting in larger handling capability. Figure 6 shows the measured transfer charges vs. channel width in the conventional double poly-silicon structure cell and in the new CCD structure cell. The new CCD structure cell gives a three times larger handling capability than the conventional structure cell at 1.2μm channel width.

4. DEVICE DESIGN AND RESULT

Figure 7 shows a schematic diagram of the new CCD. This is an interline transfer scheme. There are 1152[H]X485[V] pixels. The horizontal shift register consists of a single channel CCD, driven by three phase clocks. The vertical shift register is driven by four phase clock. Transfer electrodes are formed only by single poly-silicon layer, as shown in Fig.3(a). The space between electrodes is 0.8μm. Channel potential under the space could be controlled by applying DC voltage to the aluminum optical shield electrode. Potential pockets in the CCD buried channel could be supressed by applying -10V,-15V, and -20V to the optical shield electrode for the horizontal shift register, the part between the two shift registers, and the vertical shift register, respectively. The single layer electrode structure is simpler than the structure for the conventional double poly -silicon electrode CCD. In addition to the simplicity, this CCD is able to obtain a larger signal charge handling capability because of the shorter thermal process time for fabrication. The single poly-silicon electrode structure gives a three times larger signal charge handling capability than the conventional double poly-silicon layer structure at 1.2μm channel width, as shown in Fig.6. As a result, a 70dB dynamic range and a 700TV lines horizontal resolution are achieved.

Figure 8 is a device chip photograph. The chip size is 7.4[H]X7.4[V]mm^2. The image area measures 6.6[H]X4.8[V]mm^2, making it applicable to a 1/2" format. The pixel size is 5.7[H]X10.0[V]μm^2.

5. CONCLUSION

A 1/2" 600k-pixel interline transfer CCD image sensor, with novel single poly-silicon electrode structure, has been fabricated. In this device, the channel potential pocket under the space between CCD poly-silicon electrodes is suppressed by applying DC voltage to the aluminum optical shield electrodes. This device features high dynamic range and high resolution.

6. REFERENCES

1)J.Hynecek;IEEE TRANS,ELECTRON DEVICES,vol.ED-33,No.6,june,1986.

2)S.Manabe et al.;ISSCC Dig. Tech. Papers, (1988) pp50-51.

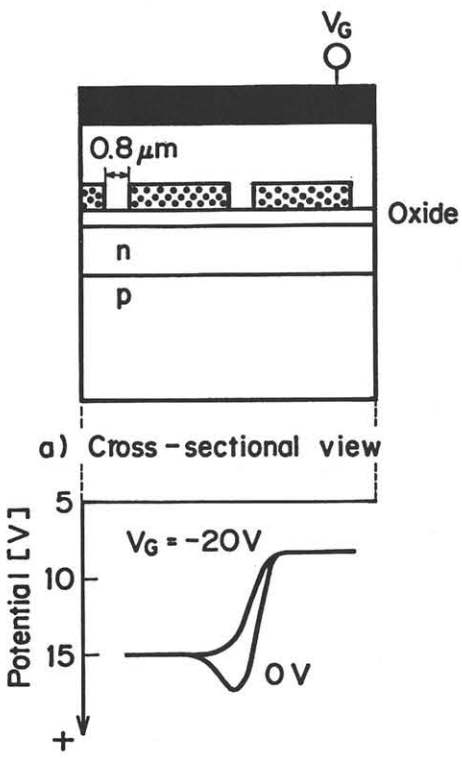
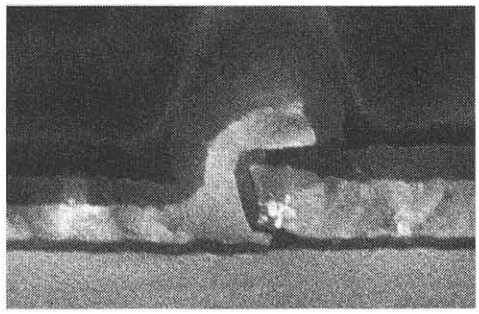
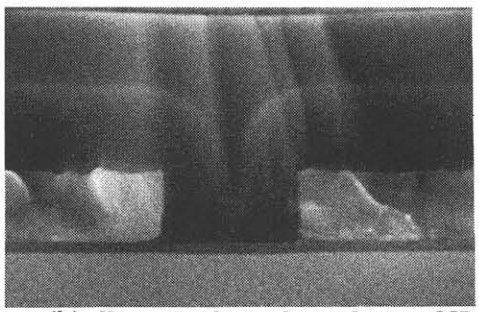


Fig.3 Single poly-silicon CCD with wide space



(a) Double poly-silicon CCD



(b) New single poly-silicon CCD

Fig.1 Cross section SEM photographs

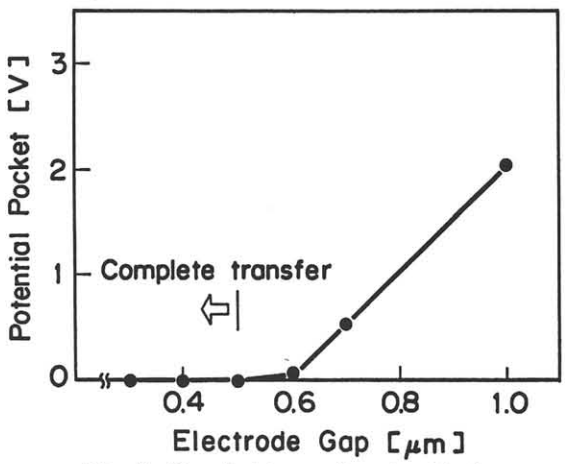


Fig.2 Simulation of potential pockets vs. electrode gap

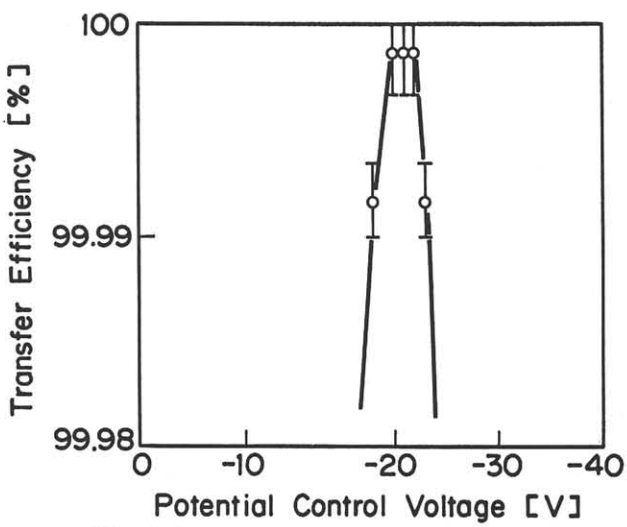


Fig.4 Transfer efficiency vs. DC voltage to aluminum electrode

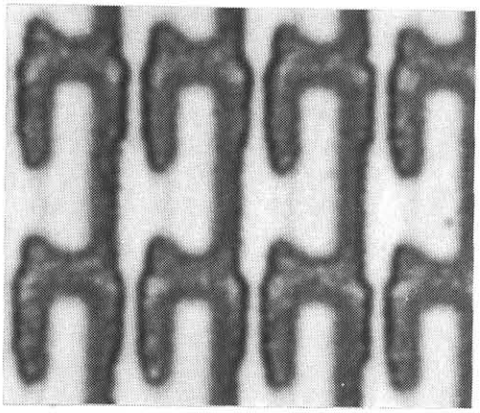


Fig.5(a) Double poly-silicon CCD cell

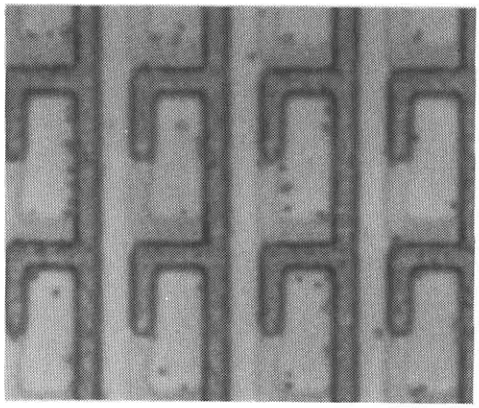


Fig.5(b) New single poly-silicon CCD cell

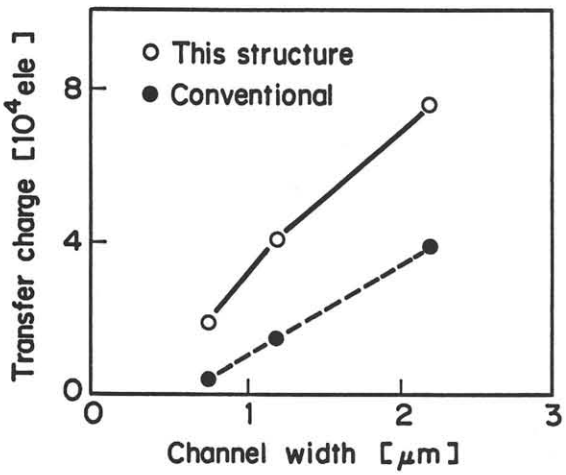


Fig.6 Transfer charge vs. channel width

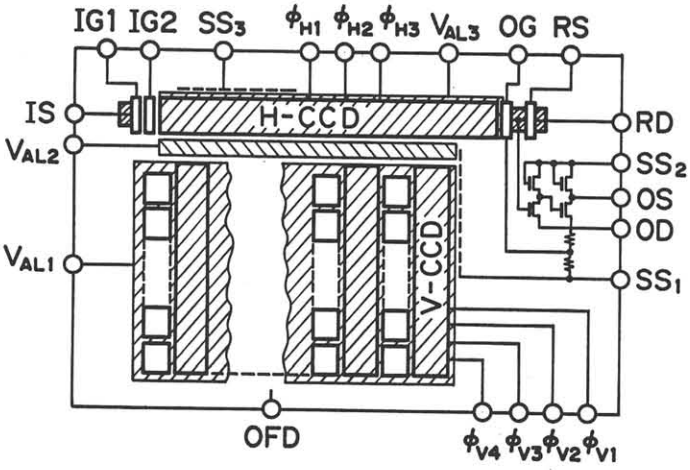


Fig.7 Device organization schematic diagram

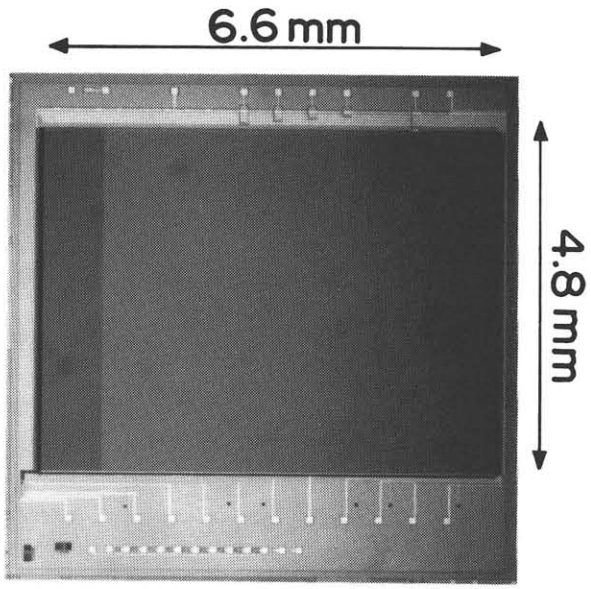


Fig.8 1/2" 600k-pixel CCD photo