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Capacitive Lag-Free CCD Imager Overlaid with an Amorphous Silicon Photoconversion Layer

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A dramatic reduction in the image lag, which is the most serius problem in the CCD imager, overlaid with an amorphous silicon photoconversion layer, was realized with a new operation. The photo-generated bias charge was injected by a light flash in the vertical blanking period, and then it was skimmed out through the field shift gate. The image lag was reduced with this operation by a factor of 1/4.

1. INTRODUCTION

An interline transfer CCD image sensor, overlaid with an a-Si photoconversion layer, features high sensitivity and a wide dynamic range. However, image lag reduction is required for this device. The image lag consists of a capacitive lag and a photoconductive lag. The capacitive lag is caused by the small subthreshold current at the field shift gate(FSG) channel and depends on storage diode capacitance. The photoconductive lag is caused by signal electron trapping in an amorphous silicon layer. It is especially important to reduce the capacitive lag, which occupies 70% in the total image lag. This paper explains a capacitive lag has been reduced, by using the new device operation, which is to reset the storage diode potential using a light flash in every field.

2. DEVICE STRUCTURE

Figure 1 shows a cross sectional view of a unit pixel. An a-Si:H film is overlaid on an interline transfer CCD(IT-CCD) scanner and acts as a photoconversion layer. The signal charges, generated in the a-Si:H film, are transported to the storage diode(SD) by an electric field in the film, and stored there. The charges are read out into the vertical CCD(VCCD) by applying an ON pulse to the FSG. They are transferred in the VCCD. In the new reset mode operation, after reading out the signal charges accumulated at the SD, the SD potential is reset by a charge injection using a light flash. On the other hand, in the conventional operation, the SD potential is not reset before beginning the signal charge storage operation, resulting in image lag appearance.

3. CAPACITIVE LAG MECHANISM

Image lag causes residual signal charge in the SD after signal read-out. Image lag [2][3]is quantitatively explained by a model based on the

MOSFET subthreshold current formula[4].

Figure 3 shows a potential profile for a unit cell in the conventional CCD. When signal charges are accumulated in the SD, SD potential ΨSD is Ψinitial.

When the field shift gate(FSG) is turned on and signal charges are read out, ΨSD is quickly changed close to FSG channel potential(ΨFSG), and the signal charge transfer speed becomes slow down. Finally, the signal charge is read out in the weak inversion region. Therefore the signal charges are not shifted completely in the limited reading out period. As the the residual charge amount depends on the quantity of signal charges accumulated in the SD before the signal reading-out, the residual charge amounts are different at every pixel. So , the residual charges are read out in subsequent reading out periods and the image lag occurs.

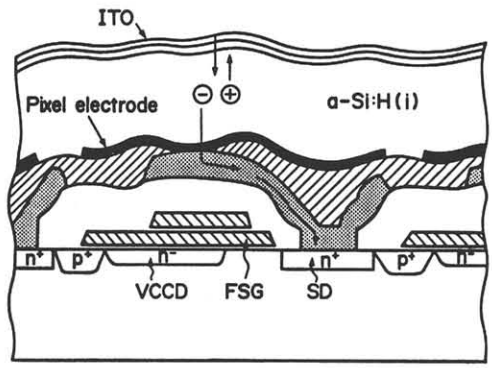

Fig.1 Unit cell cross-section

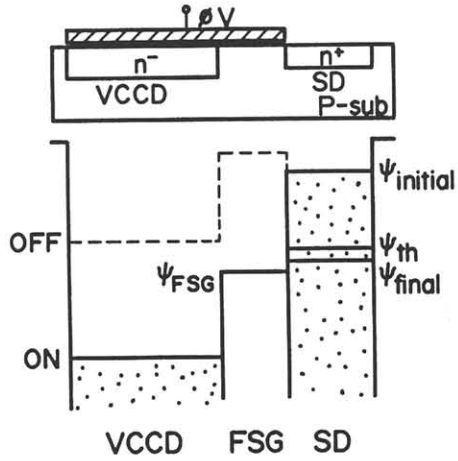

Fig.2 Unit cell cross sectional view and potential profile of conventional imager

4. IMAGE LAG-FREE MECHANISM

Figure 3 shows potential profile variation in the storage diode potential resetting(SDPR) operation period. At first, the SDs are emptied after the signal charges are read out (Fig.3(a)). The signal charges are integrated in the SD (Fig.3(b)). When the positive pulse is applied to FSG, almost all the signal charges are shifted into the VCCD. However, small signal charges could not be read and remained in SD (Fig.3(c)). This is the image lag. The FSG is turned off and the signal charges are transferred to a storage gate in the VCCD register (Fig.3(d)). Bias charges are injected to the SD by using a light flash (Fig.3(e)). The SD potential is biased to the sufficiently low potential. Subsequently, constant charges remain at the SD, due to applying the OFF pulse to the FSG (Fig.3(f)). Constant charges are transferred from the SD to the VCCD (Fig.3(g)). So , the residual charges amount the end of the transfer is approximately constant at every field. Since the residual charge amount does not depend on the initial signal charges, the SD potential before signal charges storage start is equal at every field, resulting in being capacitive lag-free. Figure 4 shows the SD transition potential during each field period. The SD potential Ψsig is the value obtained by the standard signal level, when a lamp is lit once during the storage period. When the

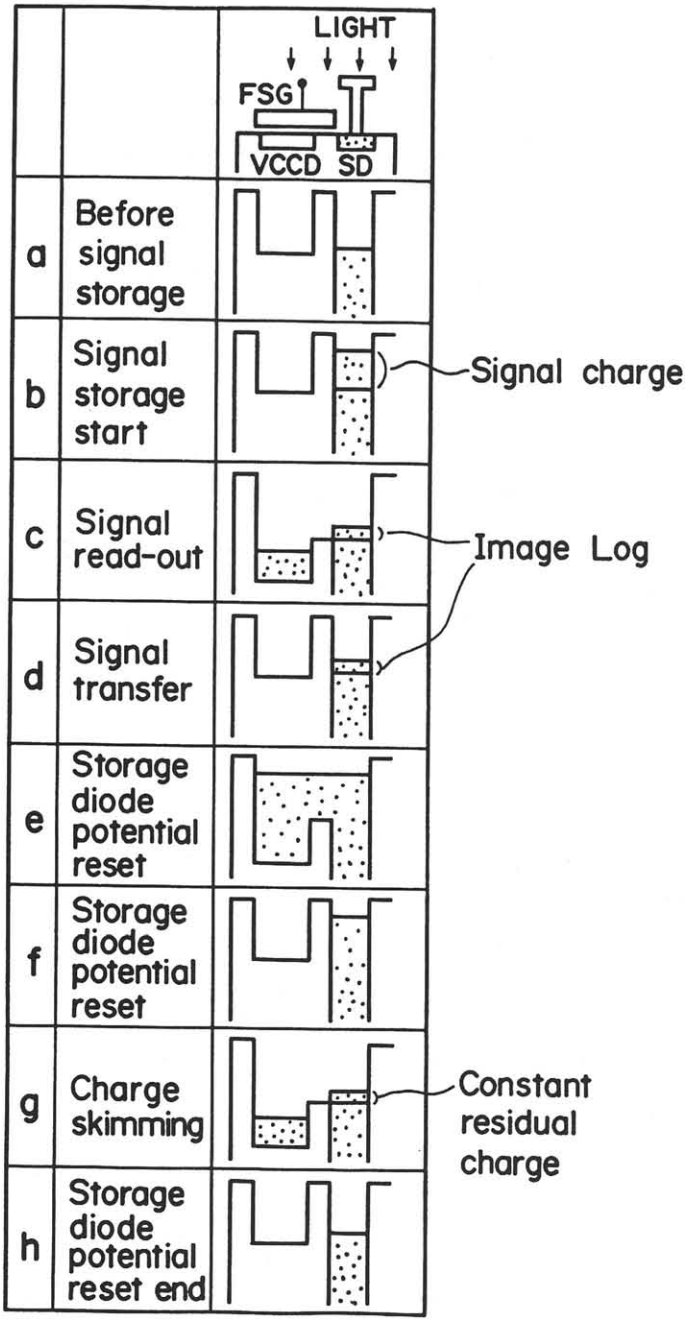

Fig.3 Potential profile

FSG is turned on, after a lamp was turned off, the SD potential increase from Ψsig to ΨR during the first field blanking period. After the signal charges are transferred, the SD potential is ΨR shown at point A. In the conventional operation mode, the SD potential is not reset at constant value during the field blanking period. So, subsequent signal charge reading-out starts from point A and ended at point B. The SD potential becomes B in the 2nd field blanking period. Image lag occurs due to the voltage difference between points A and B. The residual charge amount depends on the voltage difference. On the other hand, in the reset operation mode, the storage diode potential is reset by using a light flash in each field blanking period. For example, in the 2nd field blanking period the SD potential, which is shown at point B, is decreased to iiPR by bias charge injection, using the light flash and is reset to the potential, which is shown at point B, by shifting the bias charges out. The point B potential is equal to that at point A. The imager has no image lag, as the SD potential for all the pixels is always constant, before the signal charge storage starts.

5. EXPERIMENT

Figure 5 shows the experiment result. The image lag value, measured by using the reset mode operation, was compared with that for the conventional operation. The image lag, using the reset operation mode, was improved under the standard condition(Isig=300nA). The value was a quarter of the image lag in the conventional operation mode. Particularly, the reset operation mode utility is marked in the low illumination region. Figure 6 (a) and (b) show the reproduced images for the reset operation mode and the conventional operation mode respectively. It is evident that the image lag for the reset operation mode

is much smaller than that for the conventional operation mode.

6.CONCLUSION

The CCD imager, overlaid with an amorphous silicon photoconversion layer, was evaluated with the newly proposed operation. In this operation, the image lag charge was swept out with the injected bias charge. As a result, the image lag value at the 3rd field is reduced to 0.4%, which is a quarter of that in conventional operation.

References

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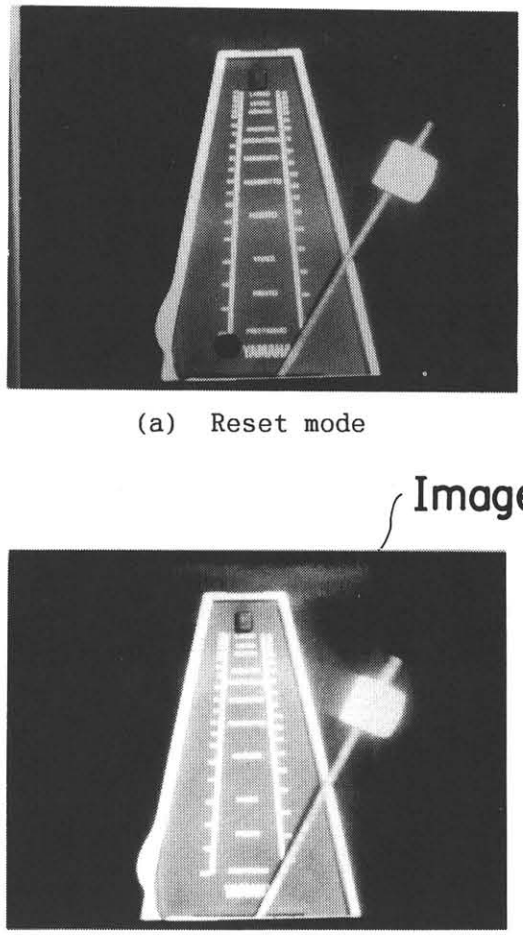

(a) Reset mode

(b) Conventional mode

Fig.6 Reproduced images obtained by reset mode and conventional mode

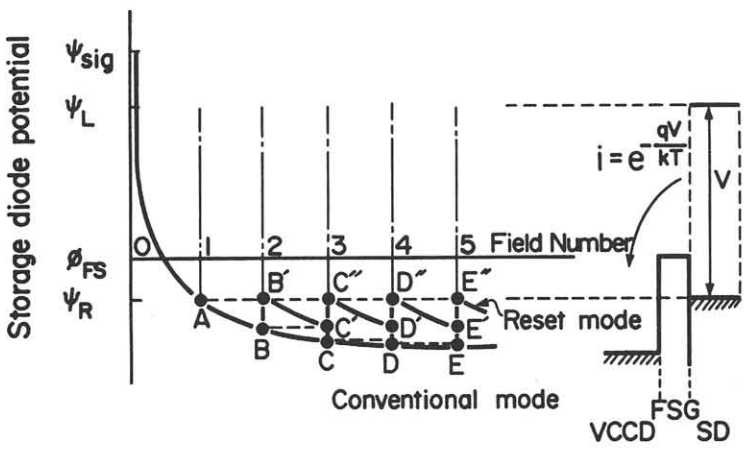

Fig.4 Storage diode potential vs. field number in reset mode and conventional mode

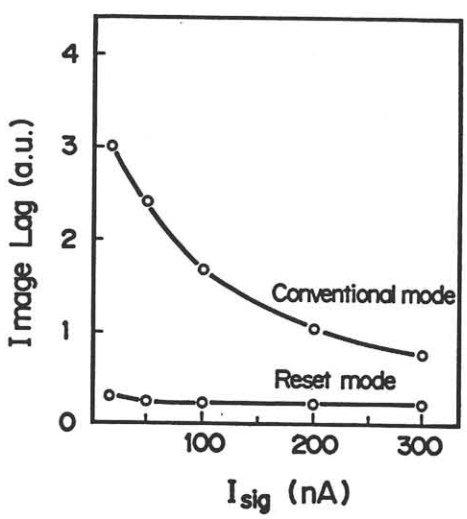

Fig.5 Decay lags vs. signal current

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