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Low Interface State Density SiO_2 on GaAs by High Quality Deposition and Ga Outdiffusion Control

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The interface states between a passivation film and an active layer have been found to exert a pronounced influence on the performance of low-noise and high-power GaAs MESFETs[1]. A number of surface treatment methods[2,3] have been attracting much recent attention as a means of improving GaAs surface and insulator/GaAs interface properties. Although these methods yield a highly stable and enduring surface, the insulator/GaAs interface property was not improved sufficiently in most cases, because interface states are always associated with defects induced by the film deposition process. This suggests the best way to achieve low interface state density (Nss) is to optimally bind an insulator on the GaAs surface without disrupting the GaAs surface. In this study, a high quality SiO_2 deposition and post annealing were investigated in an effort to enhance the interface properties. We succeeded in drastically reducing the Nss (3×10^{10} $eV^{-1}cm^{-2}$) by decreasing N and H impurities in the SiO_2 film and controlling the amount of Ga outdiffusion.

A Si-doped n-type (100) GaAs wafer was used in the study with carrier concentrations ranging from 1×10^{17} to 3.2×10^{17} cm^{-3}. SiO_2 deposition was performed by electron cyclotron resonance (ECR) PCVD using SiH_4 and O_2 source gases at below 100 °C. To compare with the SiO_2 film, SiO_XN_Y film was deposited on GaAs by the same method adding N_2. After deposition, the samples were annealed for 30 min at temperatures ranging from 300 to 800 °C. The characteristics of the SiO_2/GaAs interface were investigated by secondary ion mass spectroscopy (SIMS), Auger electron spectroscopy (AES), infrared absorption measurements (IR), and C-V measurements using Au/SiO_2/GaAs MIS diodes.

C-V curves for the SiO_2/GaAs and SiO_XN_Y/GaAs are shown in Fig. 1. The dependence of minimum Nss on the N_2 flow rate derived from the 1 MHz C-V measurements using the Terman's method is shown in Fig. 2. As the N_2 flow rate decreases, the hysteresis of the C-V curve and minimum Nss decrease. IR data indicated that the Si-H peak increased with N_2 flow rate. These results suggest that it is important to form SiO_2 film without N and H impurities to reduce Nss.

Figure 3 shows the Nss distribution of SiO_2/GaAs annealed at different temperatures (Tp). The minimum Nss decreases as Tp increases, and the minimum Nss of 1.1×10^{12} $eV^{-1}cm^{-2}$ at 300 °C decreases to 3×10^{10} $eV^{-1}cm^{-2}$ at 690 °C. This minimum value is the lowest order ever reported for a SiO2/GaAs interface. However, at 800 °C Nss increases. SIMS data show that Ga in SiO_2 film increase with Tp as shown in Fig. 4. AES data indicated that Si atoms in SiO_2 diffused to the SiO_2/GaAs interface with Tp. In the as-deposition sample, many electrically unstable Ga atoms created during the deposition process are thought to exist in the SiO_2/GaAs interface. Apparently these Ga atoms are able to easily diffuse into SiO_2 film at lower temperatures. Then Si

atoms in SiO_2 occupy the vacated positions created by Ga outdiffusion and a good SiO_2/GaAs interface is formed. However, at 800 °C many Ga atoms diffuse into the SiO_2 and excessive Ga vacancies are generated in the GaAs substrate and Nss increases. Here, it is described for the first time that Ga outdiffusion is closely related to the Nss reduction. On the other hand, post annealing process improves the SiO_XN_Y/GaAs interface property. However, the Nss decrement for SiO_XN_Y/GaAs is much smaller than that for the SiO_2/GaAs. Therefore, both of the above processes are necessary to achieve the very low-Nss. This low-Nss SiO_2 film can suppress the surface degradation of GaAs devices.

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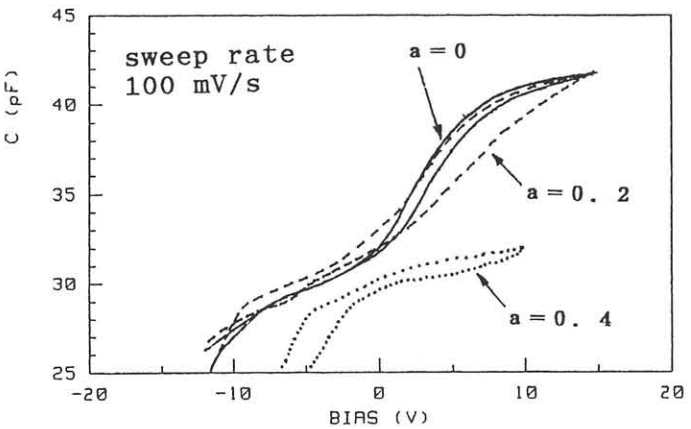

Fig. 1. C-V curves for SiO_2/GaAs and SiO_xN_y/GaAs. $a=N_2/(N_2+O_2)$

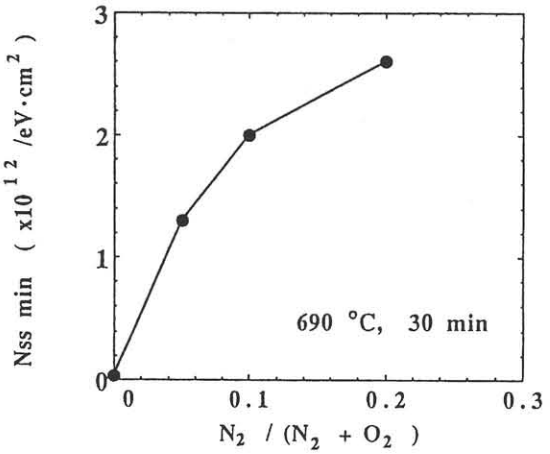

Fig. 2. Dependence of minimum Nss on N_2 flow rate. Annealing temperature is 690 °C.

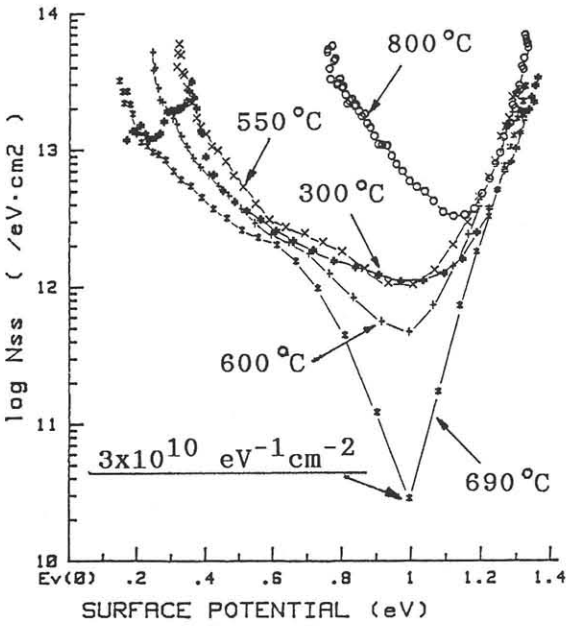

Fig. 3. Nss distributions of SiO_2/GaAs annealed at different temperatures.

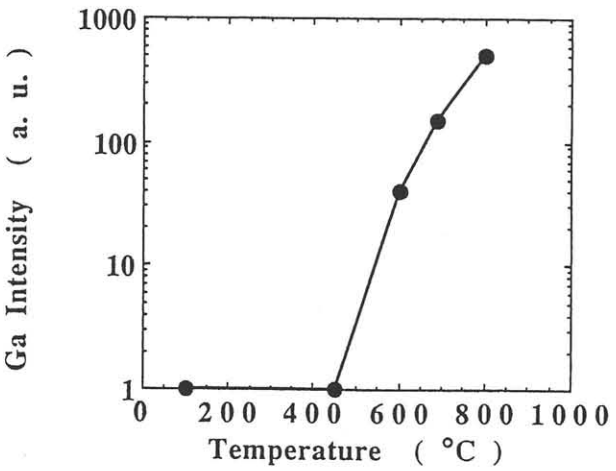

Fig. 4. Dependence of Ga intensity in SiO_2 obtained from SIMS on annealing temperature.