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A Unified Circuit Model for the Polysilicon TFT

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In the analysis of the polysilicon TFT it is reasonable to use the "distributed density of trap states" assumption [1]. In this case the system can be described by Poisson's equation in one dimension given an assumed distribution of trap states in the band gap. An analytical solution is required for a circuit simulation model. This solution, giving areal conductance, is usually found by simplification of the terms in Poisson's equation to allow the integration to be performed analytically [2]. The simplifications divide the solution into two regions: a subthreshold region in which the trapped charge dominates; and a post-threshold region in which the free charge dominates. This gives rise to a discontinuity in the conductance equations, which must be integrated once more along the channel, to give drain current and channel charge [3]. The result is a model that consists of several ill fitting equations to model the device, divided at a threshold voltage.

In this paper we propose two methods to improve the modelling of the TFT. The first involves integrating Poisson's equation numerically, given a density of trap states and other relevant material parameters including a constant mobility. The result is conductance as a numerical function of gate voltage. This function is then fitted with a polynomial in gate voltage. This may then easily be integrated to give drain current and channel charge for the TFT. A similar result has been proposed by Hack and Shur [4] for a-Si:H TFTs, but they call the polynomial a fit of variable mobility.

The second method recognizes that the data for areal conductance found by numerical integration above, may easily be found by measurement without making assumptions about the density of trap states. The resulting model accounts for the variation of mobility with gate voltage. This method of device modelling lends itself well to automated parameter extraction. Figures 1 and 2 show transfer characteristics comparing results from this model and a real device. The device is a low-temperature-process undoped polysilicon channel TFT on glass, of length 50μm and width 10μm. Note that only the electron branch of the channel current is modelled, however, a hole branch (to model the anomalous off-current) is easy to include. Figure 3 shows the output characteristics of the same device for various gate-source voltages. The figures show good agreement and a smooth progression from subthreshold to post-threshold operation.

The analyses above also yield interesting insights into the nature of the threshold voltage and mobility of the TFT. It is shown that the concept of a fixed value for the threshold voltage is not suitable for the TFT. It is also shown that the mobility of a TFT cannot be accurately assessed by the slope of the conductance characteristic.

The unified TFT circuit model proposed provides a good combination of accuracy, ease of implementation and customization.

[1] S. W. Depp, B. G. Huth, A. Juliana and R. W. Koepcke, "Theory of MOSFET operation in small grain polysilicon," in, Grain boundaries in semiconductors, Eds H.J. Leamy, G.E. Pike, and C.J. Seager, Elsevier Science Publishing Co. Inc., 1982.

[2] G. Fortunato, D. B. Meakin, P. Migliorato, "The Sub-Threshold Characteristics of Polysilicon Thin-Film-Transistors," *Japanese Journal of Applied Physics*, vol. 27, no. 11, pp 2124-2127, 1988.

[3] M.J. Izzard, W.I. Milne and P. Migliorato, "New Model for Poly-Si Thin Film Transistors for use with SPICE," *Proceedings of Materials Research Society Fall Meeting*, Boston, 1989.

[4] M. S. Shur, M. Hack, J. G. Shaw, "A new analytical model for amorphous silicon thin-film transistors," *Journal of Applied Physics*, 66(7), pp. 3371-3385, 1989.

Figure 1: TFT transfer characteristic Vds=5V

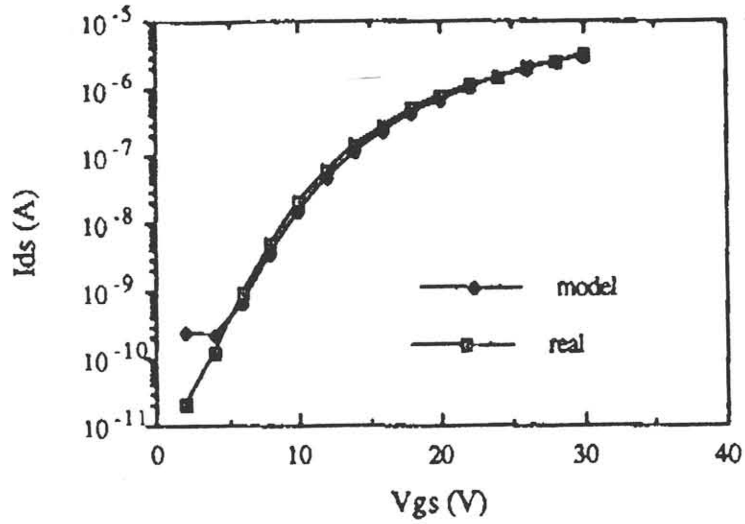

Figure 2: TFT transfer characteristic Vds=30V

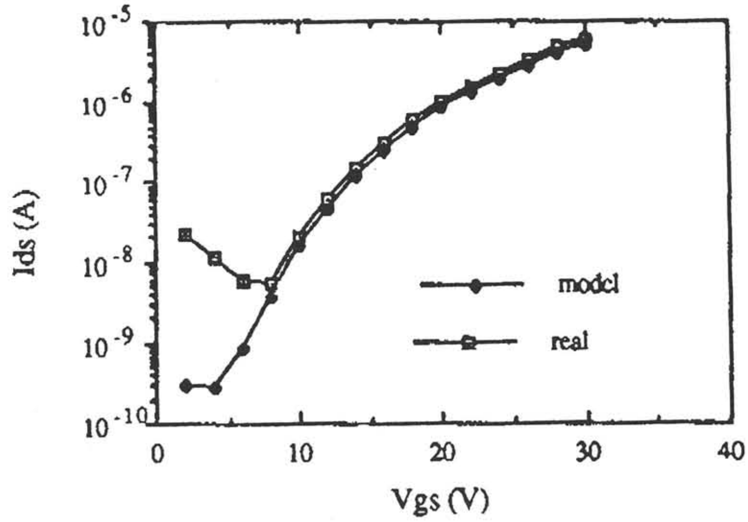

Figure 3: TFT output characteristic Vgs=20V and 30V