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A 5 nm Thick Ultra-Thin Double-Gated Poly Si TFT Using Si_2H_6 as a Source Gas

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A 5nm thick ultra-thin double-gated Poly Si TFT using Si_2H_6 as a source gas has been developed. Ultra thin Poly Si film benefits low off current(Ioff) [1] and double-gated structure improves on current(Ion).[2] In this work, Ioff less than 10fA/um and on/off current ratio(Ion/Ioff) more than 1E4 are accomplished. These characteristics could satisfy the demands for 16Mbits SRAMs with very low standby current and high cell stability.

A double-gated structure of Poly Si TFT is shown in Fig.1. Top gate(TG) is electrically connected with bottom gate(BG). A 350nm thick P^+Poly Si BG with 0.6um width was fabricated on thermally grown oxide. After side wall spacer and 150nm thick lower gate oxide formation, ultra thin Si film as a TFT body was deposited at 500C by conventional LPCVD system using Si_2H_6 as a source gas. A 35nm upper gate oxide was grown by LPCVD at 800C. A 150nm thick P^+Poly Si TG formation just on the BG was followed by B^+ ion implantation at a dose of 4E14cm^{-2} to form source and drain regions, when TG with photo resist acted as a self-aligned mask as shown in Fig.2. CVD oxide and BPSG were deposited and annealed at 950C in N_2 for 30min. After contact hole opening and Al-Si metallization, devices were sintered at 420C. Hydrogenation was not carried out in this process.

Fig.3 shows TEM photograph of 5nm ultra thin Si film as a TFT body. Its grain size is about 25nm as the same as 5 times of film thickness. In Si LPCVD, with decreasing deposition temperature nucleus density increases and island growth is suppressed. As a result, ultra thin continuous film grows. Because Si_2H_6 is dissociated at lower temperature than that of conventional SiH_4, Si_2H_6 is attractive source gas for the well-controlled growth of ultra-thin continuous Si film. Fig.4 shows drain current(Ids) characteristics of 5nm ultra-thin double-gated TFTs with various TG width(Wt) at drain voltage(Vd)=-4V, in which BG width(Wb) of all is 0.6um. By thinning Poly Si to 5 nm, Ioff drastically decreases and reaches to 4fA/um.

Fig.5 shows Ioff, Ion and Ion/Ioff of 5nm thick ultra-thin double-gated and single gate TFTs with a 0.6um wide BG as a function of Wt. Single gate TFTs have the same structure as double-gated ones, but their TG are only biased. Both of Ion and Ioff decrease in Wt between 1.0 and 1.6um. Fortunately, Ion of double-gated TFTs is larger than that of single gate TFTs. This reduction of Ids is caused by vertical offset structure for TG as shown in Fig.2, where TG is slightly wider than BG. At the time of B^+ ion implantation to source and drain region, TFT body along side wall of BG is not implanted because ion direction is parallel to it, which results in offset formation. In the case of single gate TFTs, offset region behaves only resistor, while in the case of double-gated TFTs, it is modulated by BG and Ion is improved. Because of thicker side wall spacer than that of gate oxide on BG, electric field in the offset region is weak but its

effectiveness is sufficient for high Ion/Ioff.

In conclusion, 5nm ultra thin Poly Si can be deposited by using Si_2H_6 as a source gas. Using it, double gated TFTs with vertical offset region for top gate have accomplished Ioff as low as 4fA/um and Ion/Ioff as high as 3E4. Ultra-thin double-gated TFTs will promise 16Mbits SRAMs.

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REFERENCES

[1]T.Hashimoto et al.,Ext. Abs. the 21st Conf. SSDM(1989), p97
[2]A.O.Adan et al.,Symp. on VLSI Tech. Dig.(1990), p19

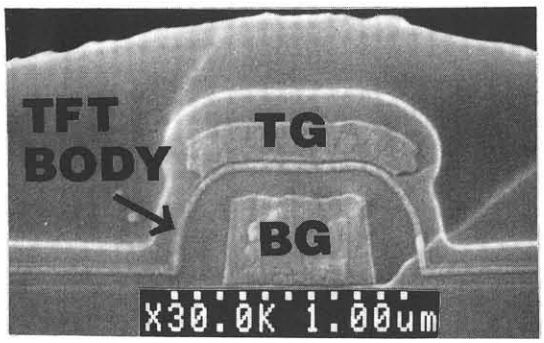

Fig.1 SEM photograph of double-gated Poly Si TFT structure

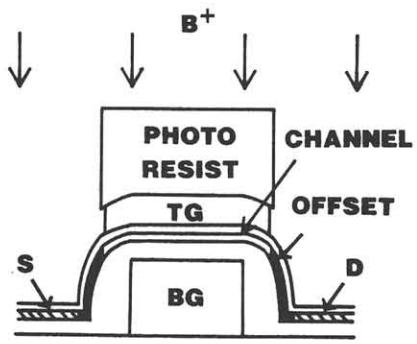

Fig.2 Schematic cross-section of vertical offset structure

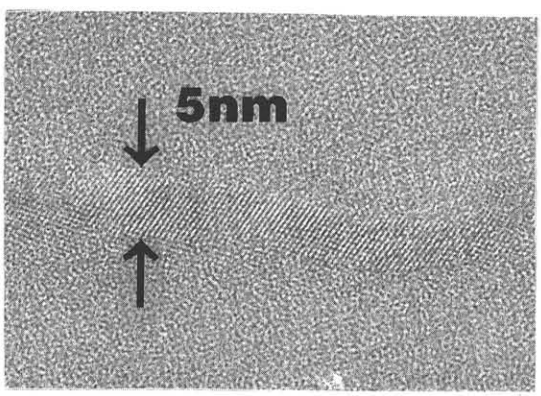

Fig.3 TEM photograph of 5nm ultra thin Poly Si film

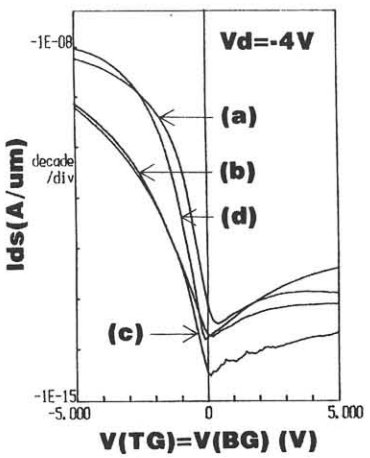

Fig.4 Ids characteristics of ultra-thin double-gated TFTs with various Wt
Wb=0.6um, Vd=-4V
Wt:(a)0.8um, (b)1.0um
(c)1.4um, (d)2.0um

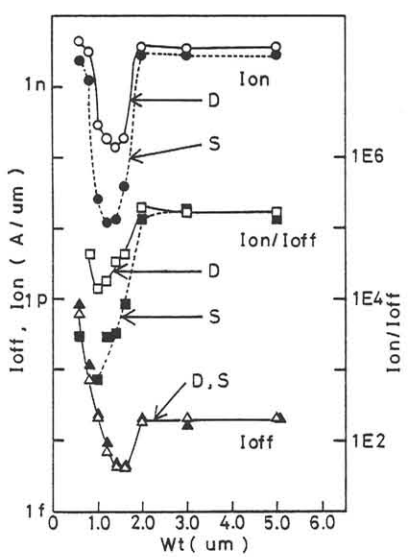

Fig.5 Ioff, Ion and Ion/Ioff of double-gated(D) and single gate(S) TFTs as a function of Wt at Vd=-4V