

Invited**Surface Emitters and Heteroepitaxy OEICs for Optical Interconnection**

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This talk will describe an approach to solving the interconnect problem between Si integrated circuits in electronic computers and other systems. The number of transistors per chip has been doubling every two years for the past twenty years, a remarkable increase of more than a factor of 1000 with no end in sight. The limitations to this progress do not appear to be on the chip, but in the packaging and electrical interconnects.

Today's integrated chips have two to 200 leads. By 1995, this figure will climb to 1000 for the most complicated chips. The reliability and high cost of 1000 lead packages has led us to look at optical interconnects between chips as an alternative. Our analysis, which we will describe, shows that an optical interconnect consisting of a multiplexer to

get to high data rate connected to a laser transmitter for single channel output and optical receiver followed by a demultiplexer for single channel input is advantageous even for today's Si integrated chips. If the 100 communications pins of the total 150 pins on the new Intel 486 microprocessor were replaced by a single 2.1 Gbit/sec optical input and output channel, then the chip area and the overall power could be decreased by 20% with two-thirds less wire bonds and pins on the package plus having the flexibility and immunity from ground loops, EMI and RFI, which optics brings.

The steps taken to realize such circuitry including integrated receivers and grating surface emitting lasers at Sarnoff will also be discussed.

